

- ## GX701LX Block Diagram

The diagram illustrates the system architecture centered around the **Comet Lake H-Processor (HM370)**, which is a **BGA Quad Core** processor. The architecture is color-coded by function:

- Blue:** I/O and Data Paths (e.g., USB, PCIe, SATA, Display, Audio).
- Green:** Power Management (e.g., Voltage Regulators, PMICs, DC-DC converters).
- Red:** Thermal Management (e.g., Thermal Sensors, Thermal Diodes).
- Purple:** Other specialized functions (e.g., USB Type-C, CC).

Key Components and Connections:

- Memory:** DDR4 SO-DIMM X1 (Page 16) and DDR4 On Board Memory X1 (Page 14-15) are connected via **DDR4** to the CPU.
- Storage:** PCIe Gen3 x4 SSD (Page 40) is connected via **PCIe #9-12** to the CML PCH-H.
- Graphics:** The CPU connects to the CML PCH-H via **DMI3.0 x4**. The PCH-H connects to the DP MUX TS3DV642 (Page 69) via **eDP** (Page 70-72, 77-79) and to the Level Shifter SN75DP159 (Page 48) via **DDI**. The DP MUX connects to the LCD Panel (eDP) (Page 45), and the Level Shifter connects to the HDMI (Page 45).
- Audio:** The CML PCH-H connects to the Azalia Codec Realtek ALC3288-CG (Page 36) via **HDA**. The Azalia Codec is connected to the INT. SPK (Page 39), INT. DMIC (Page 45), and EXT MIC (On FPC) via the Audio Jack (Page 37).
- USB and I/O:** The CML PCH-H connects to the USB3.0 and USB 2.0 ports (Page 20-29) via **USB3.0** and **USB 2.0**. It also connects to the USB Charging Controller TPS2544 (Page 38) and the USB3.0 redriver P3EQX1002B1ZLEX+FDX (Page 52) for USB Port 1, USB Port 3, and USB Port 4. The CML PCH-H also connects to the DP TUSB1046A (MUX) (Page 47) via **DP** and to the USB Type-C (Page 46) via **USB**. The USB Type-C is connected to the TP565993AC (PD+CC) (Page 46) via **CC**.
- Power Management:** The CML PCH-H connects to the TBT_Titan Ridge (Page 11) via **PCIe #17-20** and to the TP565987(PD) (Page 12) via **CC**. The TBT_Titan Ridge is connected to the USB Type-C (Page 12) via **USB**. The TP565987(PD) is connected to the USB Type-C (Page 12) via **CC**.
- Other Components:** The CML PCH-H connects to the Debug Conn. (Page 44) via **I2C**, the Touch Pad (Page 31) via **I2C**, the SPI ROM (Page 38) via **SPI**, and the EC ITE IT5125VG/CX (Page 30) via **LPC**. The EC is connected to the Debug Conn. (Page 44) via **I2C** and to the Touch Pad (Page 31) via **I2C**. The EC is also connected to the SPI ROM (Page 38) via **SPI** and to the Debug Conn. (Page 44) via **LPC**. The CML PCH-H connects to the WiFi/WiMax+BT (Page 53) via **CNVi**.
- Thermal Management:** The CML PCH-H connects to the CPU XDP (Page 7), PCH XDP (Page 28), Reset Circuit (Page 32), Thermal Sensor (Page 40), PWM Fan (Page 50), LEDs (Page 54), DC & Battery (Page 60), Skew Holes (Page 60), Power Protect (Page 60), and EMI Caps (Page 60).

VCORE+VCCSA+VCCGT	Page 80,Page 81
+1.05VSUS	Page 83
+1.8VSUS	Page 84
+1.2V/+2.5V	Page 86
System (+3VA/+5VA)	Page 87
Load Switch	Page 88
Power Charger	Page 89
VGA CORE (+NVDD)	Page 91,Page 92
PD Charger	Page 93
+FBVDDQ	Page 94
ChargePump	Page 95
+12VS_FAN	Page 96
IPC	Page 98

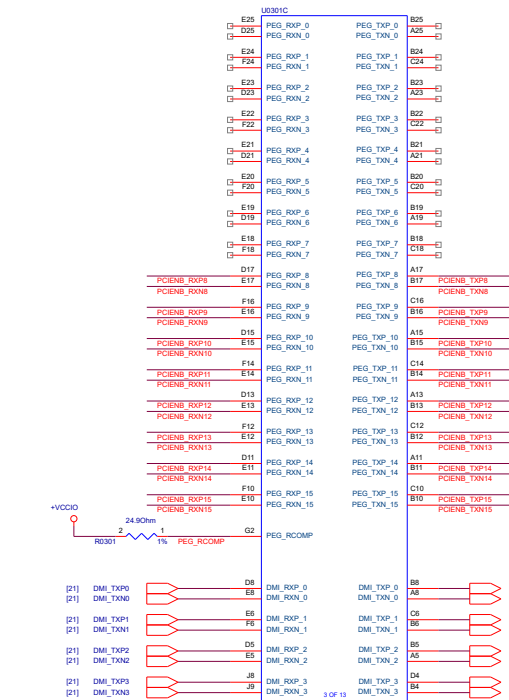
IT8995 GPIO

N501VW Setting

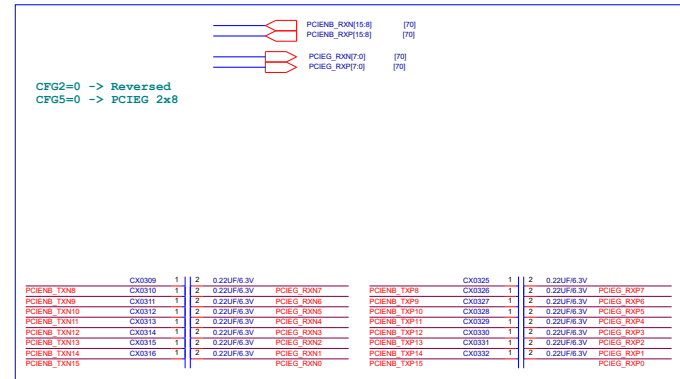
	Function	SAC
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		Project Name	
		GX701	
Title :		System Setting	
Date :	Doc# :	ASUSTek COMPUTER INC.	Engineer: FF

PCIEG

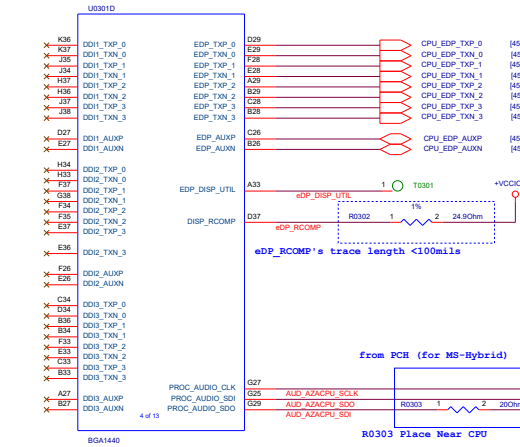


R0.1-25

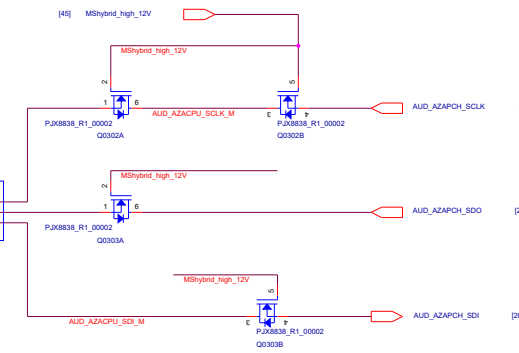


Main Board

Display



AUX of EDP



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Table 81. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processo r	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	1	1	1	1	1	1	9	8	7	6	5	4	3	2
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

Notes: 1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.

2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:

- Connect lane 0 of 1st device to lane 0.
- Connect lane 0 of 2nd device to lane 8.
- Connect lane 0 of 3rd device to lane 12.
- For example:
 - When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane12.

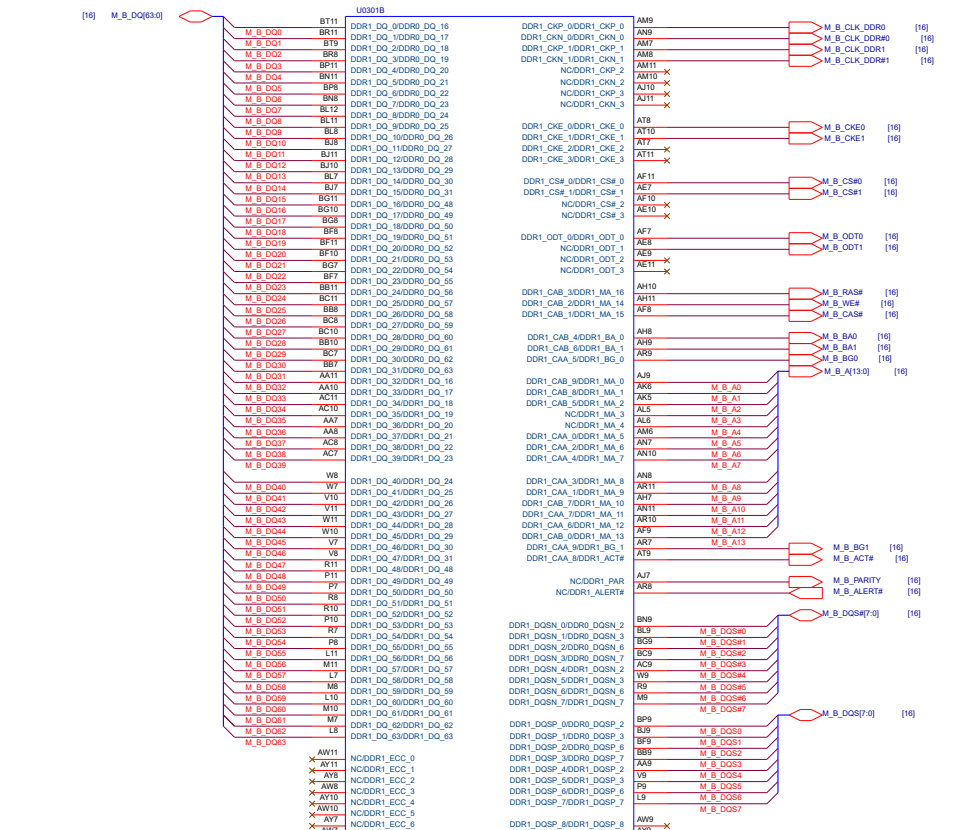
Refer to CML-H PDG P.339 (Doc.611586)

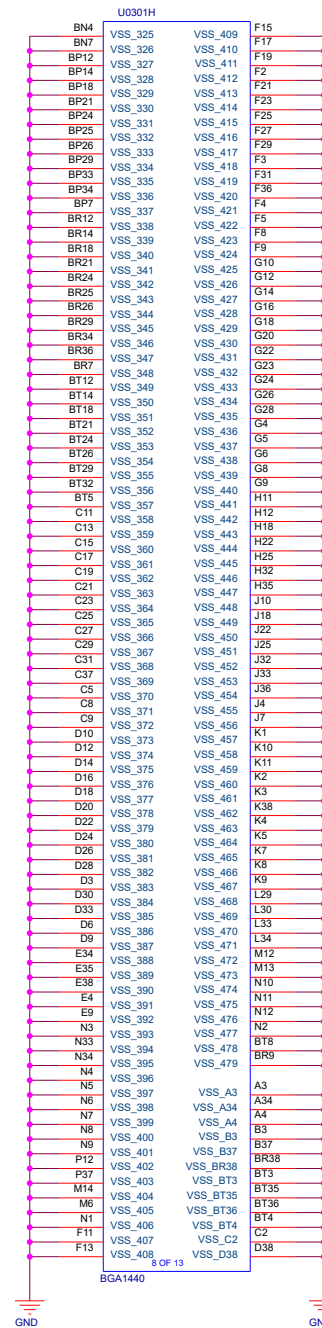
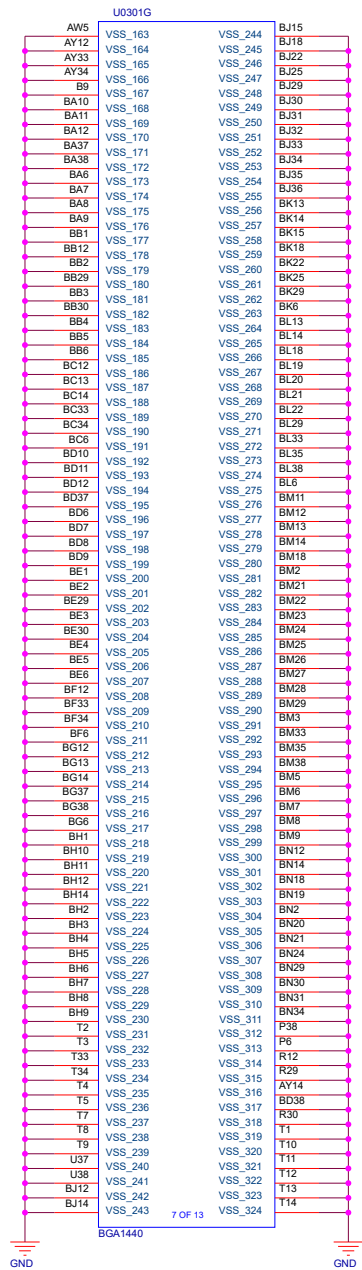
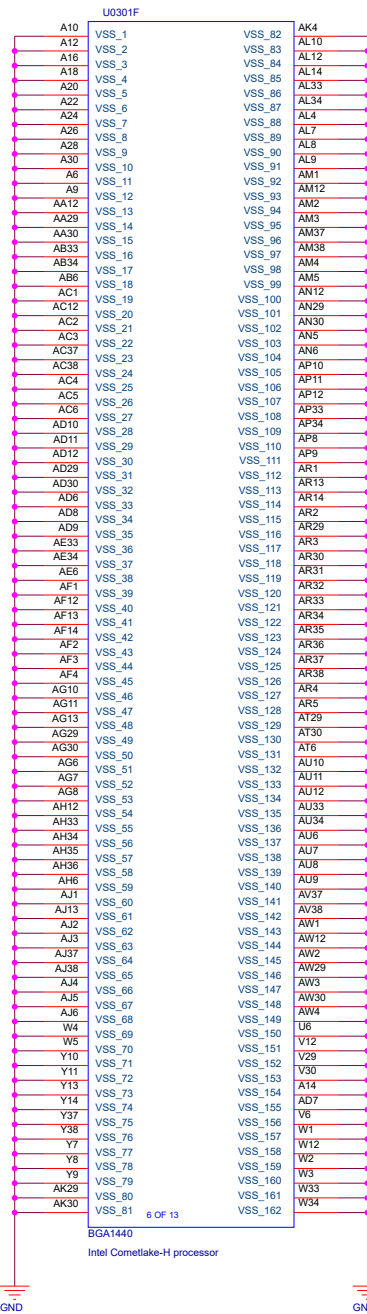
Disabling and Termination Guidelines for the Intel High Definition Audio Interface and the Intel Display Audio Interface

When the Intel HD Audio interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI on the CPU need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO on the CPU can be left unconnected. The Intel Display Audio pins on the PCH may be left disconnected.

Main Board

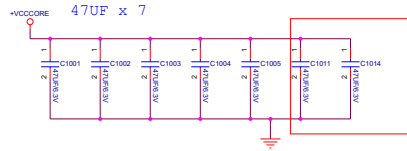




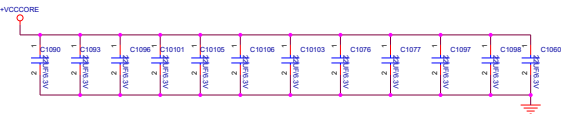
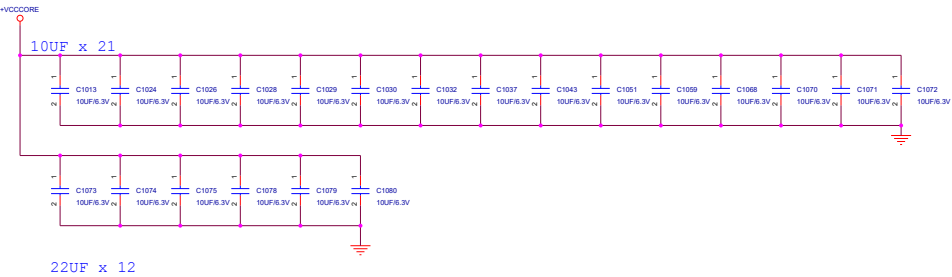
CPU XDP

+VCCORE near CPU

Increase 47UF x 2 for CML

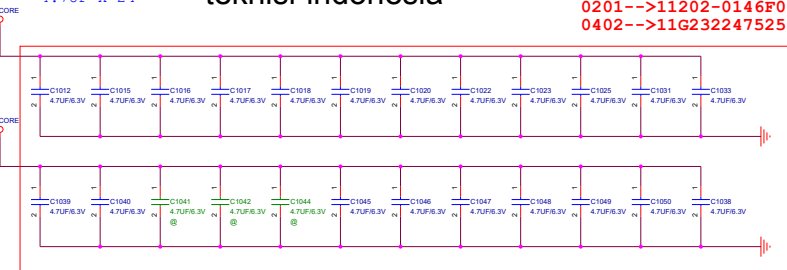


+VCCORE DECAPS Place Back Side (TOP)



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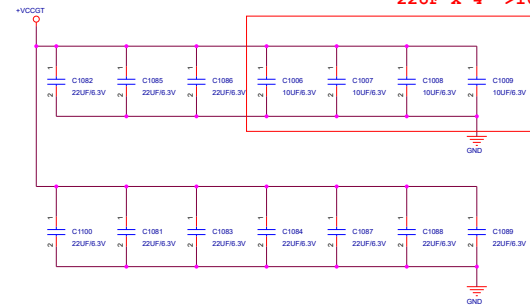
1UF x 24-->4.7UF for CML
0201-->11202-0146F000
0402-->11G232247525360



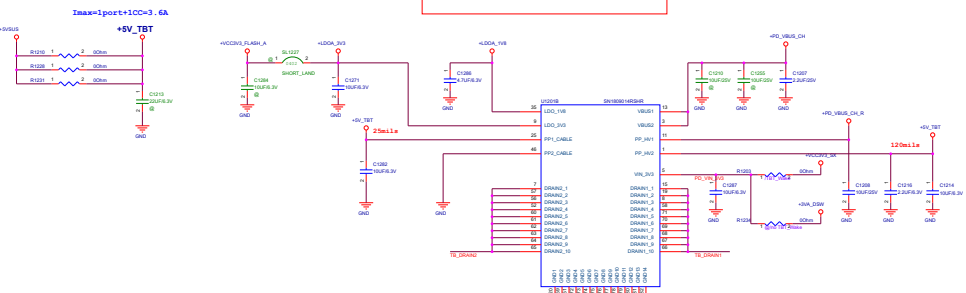
+VCCGT cap near CPU

22uF x10
10uF x4

22UF x 4-->10UF for CML



BOM修改為TPS987DDJ料號
(P/N:06050-00920000)



SW1_MASSIVE Pinout Description

SW1 connect RESET, RESET signal will be asserted to SW1 and assert a RESET signal to TBT.

Notice

Connect to SW1 only All (VPL Platform)
connect to SW1 only for TBT battery reset support
connect to SW1 only for TBT battery reset support
SW1 - No Reset, connect to SW1 only assert
SW1 - Reset, connect to SW1 only assert

TPS65987 (TPS65988 價格不一樣)

IC1 address	R1219	R1219+R1230	R1219+R1247	R1219+R1209
IC1_C1_ADDR	001b	001b	010b	011b
IC1_C2_ADDR	100b	101b	110b	111b

Table 2. PC Default Unique Address IC1 - Port 1

Default PC Unique Address	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	0	1	0	1	0	1

Note 1: Any bit is available for each port independently providing firmware override of the PC address.

Table 3. PC Default Unique Address IC1 - Port 2

Default PC Unique Address	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	0	1	0	1	0	1

Note 1: Any bit is available for each port independently providing firmware override of the PC address.

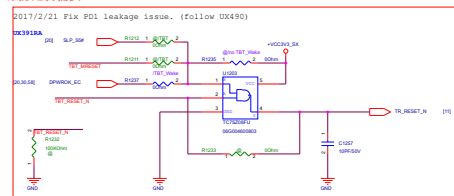
For the IC2 interface, the unique PC address is a feed value as shown in Table 4 and Table 5.

Table 4. PC Default Unique Address IC2 - Port 1

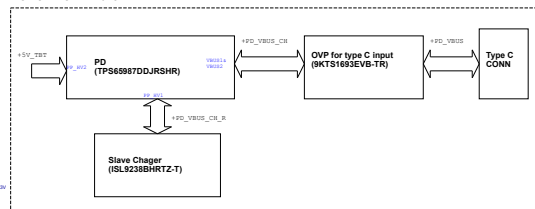
Default PC Unique Address	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	1	1	1	0	0	0

Note 1: Any bit is available for each port independently, providing firmware override of the PC address.

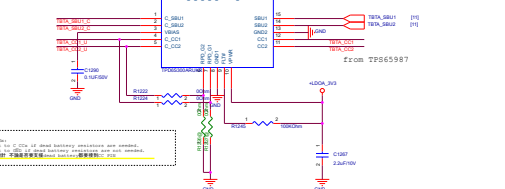
確認是否需



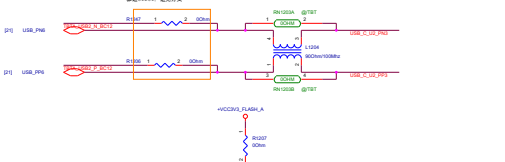
Power Flow Chart



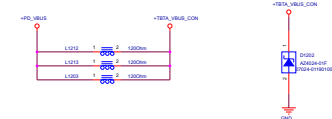
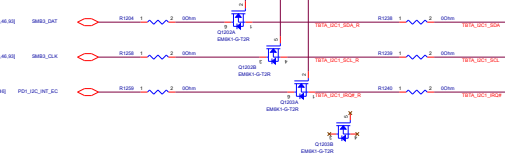
To Connector



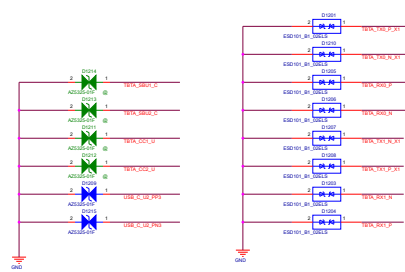
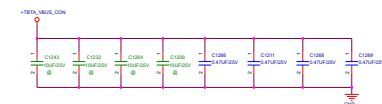
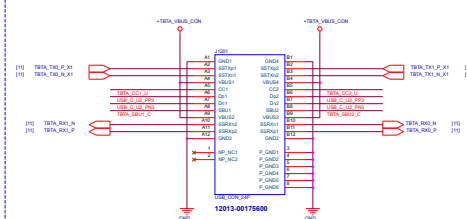
FROM PCB




FROM EC

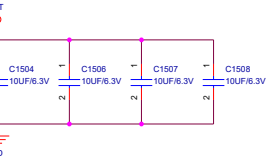


TYPE-C Connector

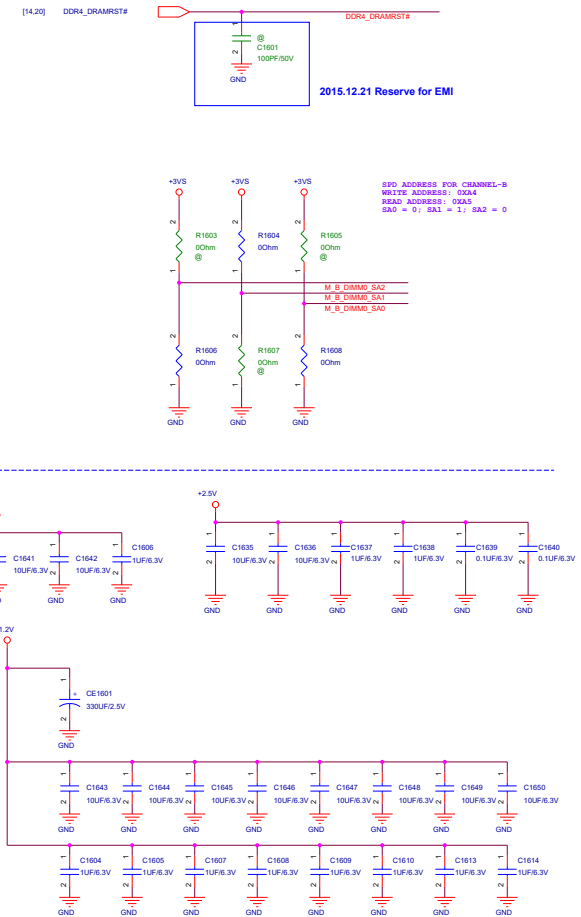


<Variant Name>

		Title : DDR4_TERMINATION	
ASUSTeK COMPUTER INC.		Engineer: EE	
Size Custom	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 13 of 103	



Main Board



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

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<Variant Name>


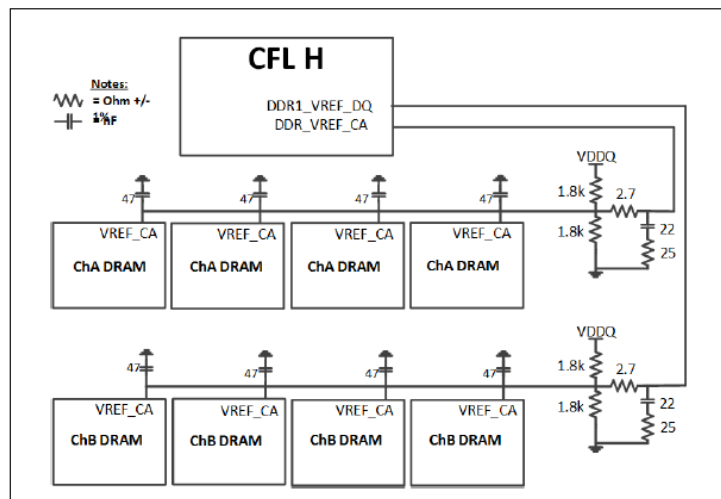
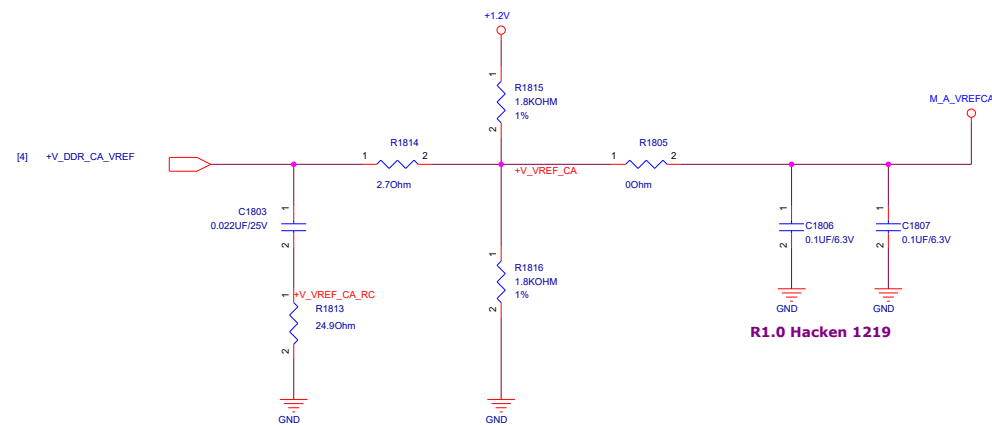
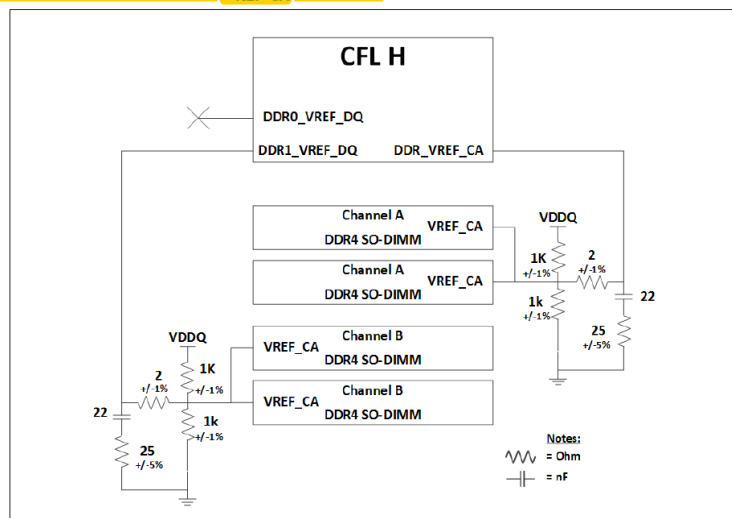
		Title : NB_****	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 17 of 103	

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

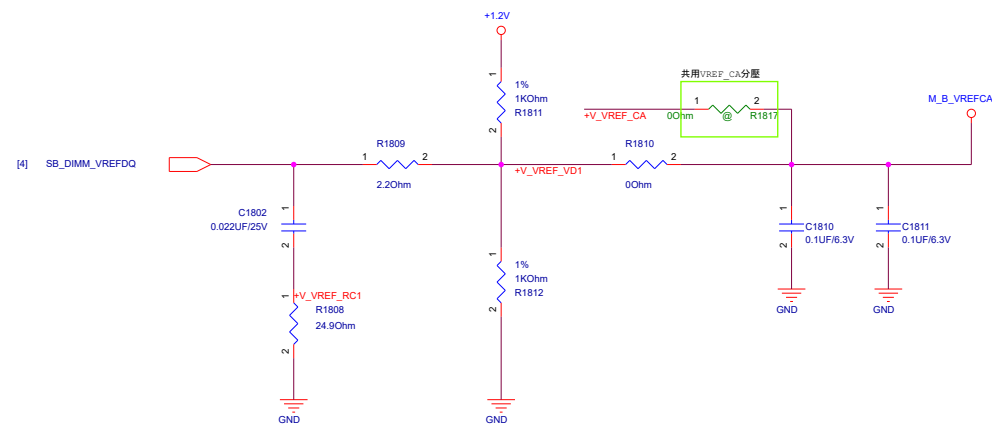
Memory Down Vref




R1.0 Hacken 1219

Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

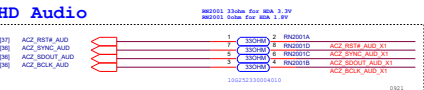
SO-DIMM1 Vref



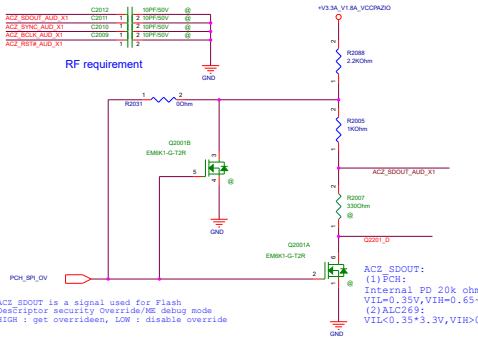
<Variant Name>

		Title : *****	
ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 19 of 103	

HD Audio

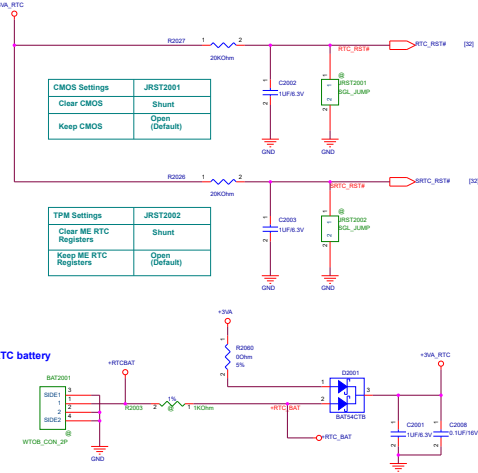


RF requirement

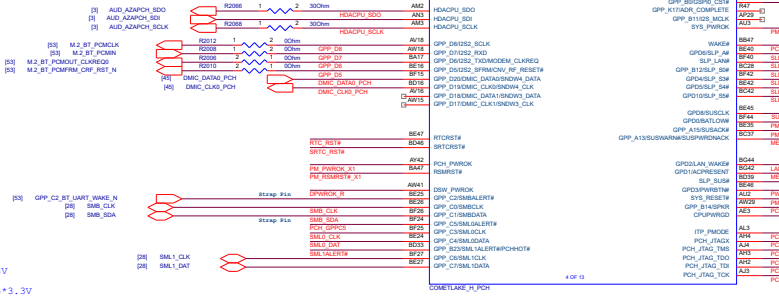
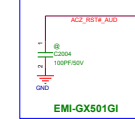


ACZ_RSTA_AUD is a signal used for Flash Overwrite security Override/ME debug mode HIGH : get overridden, LOW : disable override




Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAG	+3VA	+3VA_BC	
	+3VSW	+3VSUS	+3VSUS_PCH	+V3_V1_VA_VCCST
		+3VS		

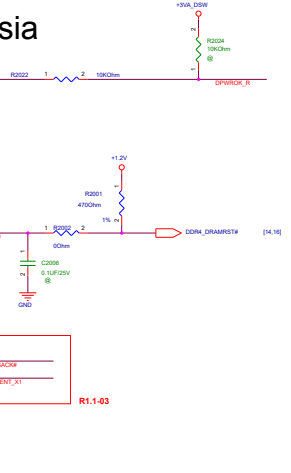
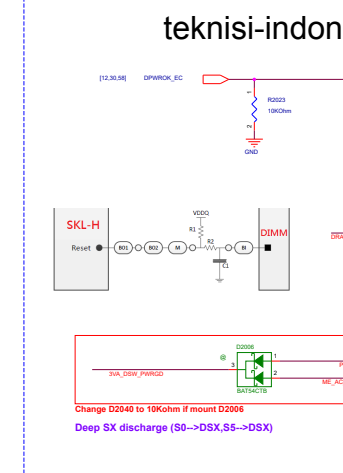
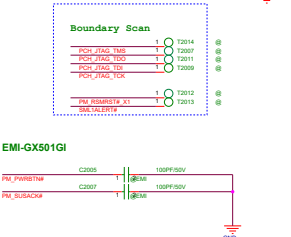
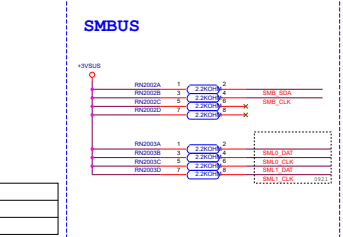


1st : 12017-0002000
2nd : 12017-0002000
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI R1220 3V



Power failure solution (S0->G3,S5->G3):

eSPI or LPC	TLS Confidentiality		Top Swap Override
			
PCH_GPPC5: weak internal pull down	PU	Enable	PCH_GFPB14: weak internal pull down
PD	eSPI	Enable	PD
PD	LPC (default)	Disable (default)	PD
		Disable (default)	PD



1st : 12017-0002000
2nd : 12017-0002000
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI R1220 3V

1st : 12017-0002000
2nd : 12017-0002000
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI R1220 3V

QX501G1 PCIE/SATA Function define

CHL HM370

Function	Function
MSIO Capabilities	
PCIE0 (from GPU)	
PCIE01- USB3.1007	
PCIE02- USB3.1008	
PCIE03- USB3.1009	
PCIE04- USB3.1010	
PCIE05	
PCIE06	
PCIE07	
PCIE08	
PCIE09	
PCIE10	PCIE* SSD
PCIE11- SATA-0a	
PCIE12- SATA-1a	
PCIE13- SATA-0b	
PCIE14- SATA-1b	
PCIE15 / SATA02	
PCIE16 / SATA03	
PCIE17 / SATA04	
PCIE18 / SATA05	
PCIE19 / SATA06	
PCIE20 / SATA06	
PCIE21	TBT (M4)
PCIE22	
PCIE23	
PCIE24	

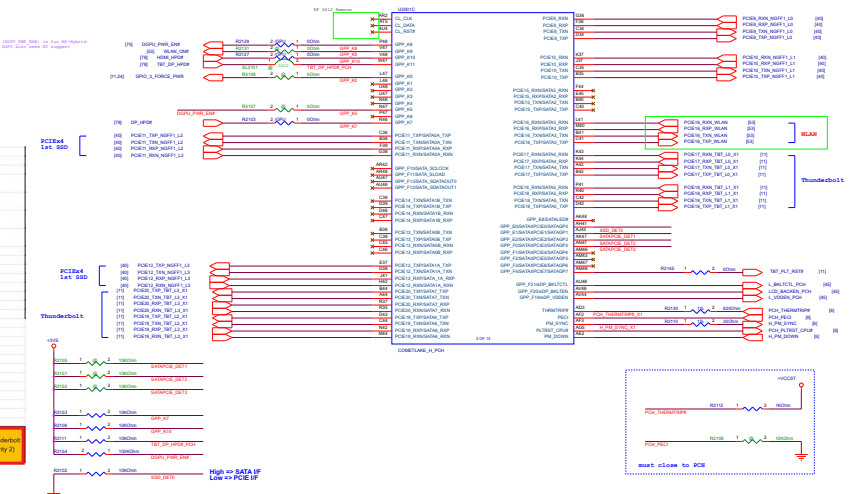
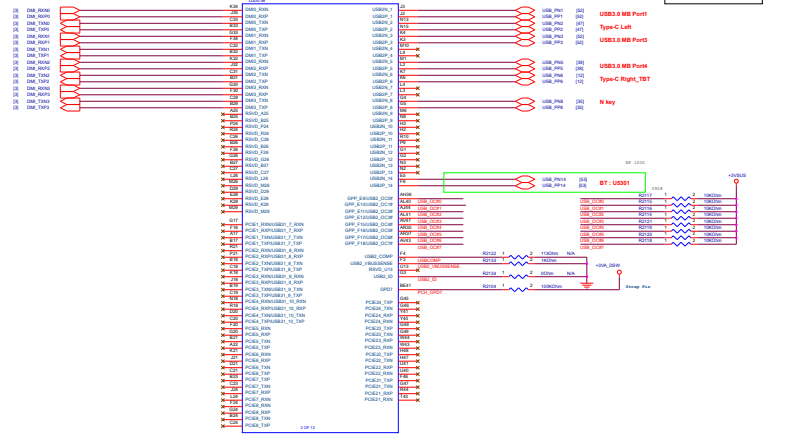
Function	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	WLAN
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIe SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting QX501G1 USB Function define

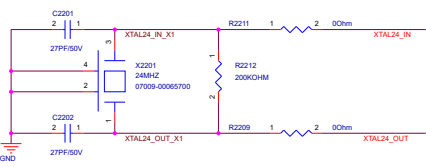
CHL HM370

Function	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	USB3.1007
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

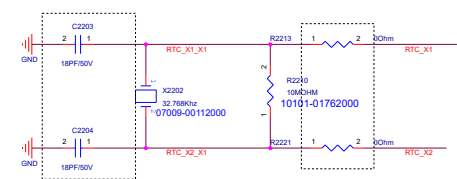
FBIO	HM370	QX501G1	CM246	RSIO	Device Assign
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1		
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2		
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3		
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4		
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5		
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6		
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7		
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8		
8	USB3.1 Gen1 #9	USB3.1 Gen1 #9	USB3.1 Gen1 #9		
9	USB3.1 Gen1 #10	USB3.1 Gen1 #10	USB3.1 Gen1 #10		
10	NA	PCIe #0	PCIe #0		
11	NA	PCIe #1	PCIe #1		
12	NA	PCIe #2	PCIe #2		
13	NA	PCIe #3	PCIe #3		
14	NA	PCIe #4	PCIe #4		
15	PCIe #5	PCIe #5	PCIe #5		
16	PCIe #6	PCIe #6	PCIe #6		
17	PCIe #7	PCIe #7	PCIe #7		
18	PCIe #8	PCIe #8	PCIe #8		
19	PCIe #9	PCIe #9	PCIe #9		
20	PCIe #10	PCIe #10	PCIe #10		
21	PCIe #11	PCIe #11	PCIe #11		
22	PCIe #12	PCIe #12	PCIe #12		
23	PCIe #13	PCIe #13	PCIe #13		
24	PCIe #14	PCIe #14	PCIe #14		
25	PCIe #15	PCIe #15	PCIe #15		
26	PCIe #16	PCIe #16	PCIe #16		
27	PCIe #17	PCIe #17	PCIe #17		
28	PCIe #18	PCIe #18	PCIe #18		
29	PCIe #19	PCIe #19	PCIe #19		
30	PCIe #20	PCIe #20	PCIe #20		
31	PCIe #21	PCIe #21	PCIe #21		
32	PCIe #22	PCIe #22	PCIe #22		
33	PCIe #23	PCIe #23	PCIe #23		
34	PCIe #24	PCIe #24	PCIe #24		



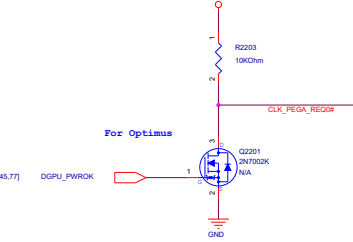
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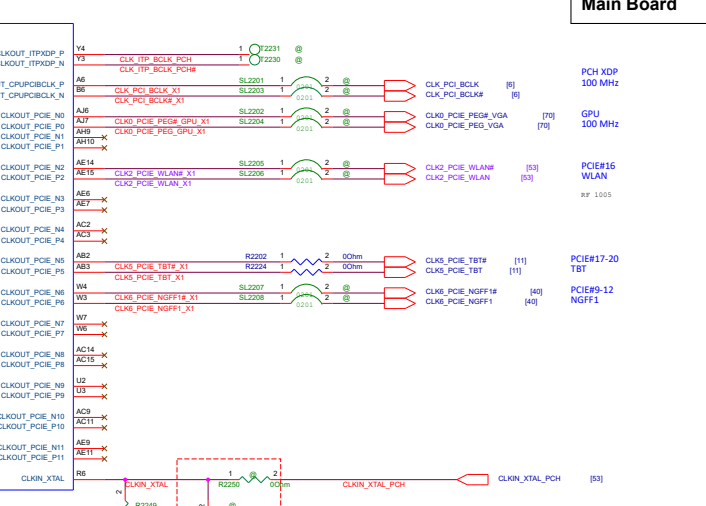
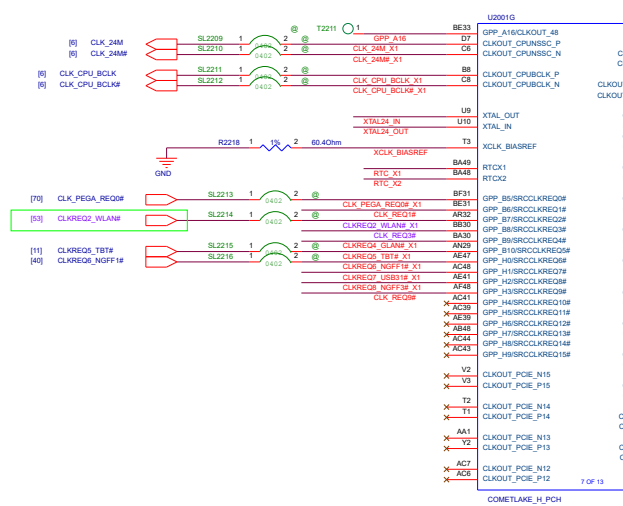
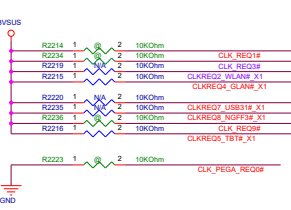
RTC CRYSTAL 32.768KHz



DGPU CLKReq#



PCH CLKREQ Setting:



MB USB3.0 : N/A

USB3.0 Type C : Left

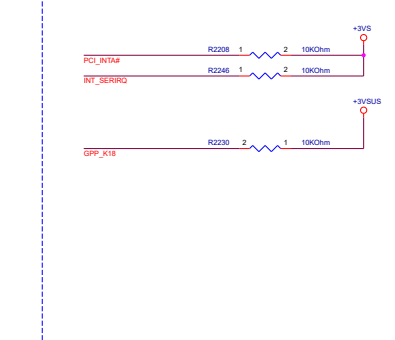
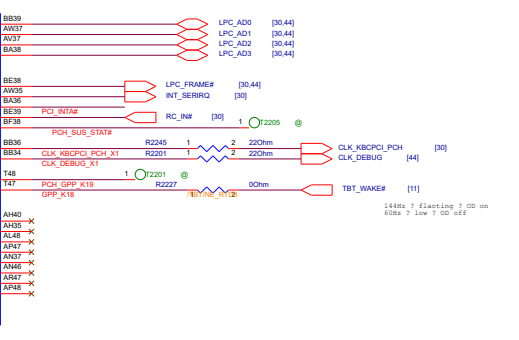
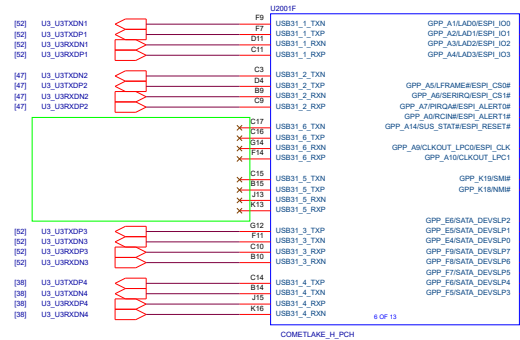
EE 0709 Remove

USB3.0 Type C : Right

USB3.0 Type C : Right

USB3.0 Port3 : N/A

USB3.0 Port4 : Left



HPD0 to DP
HPD1 to HDMI
HPD2 to TBT
HPD3 to VGA
HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected

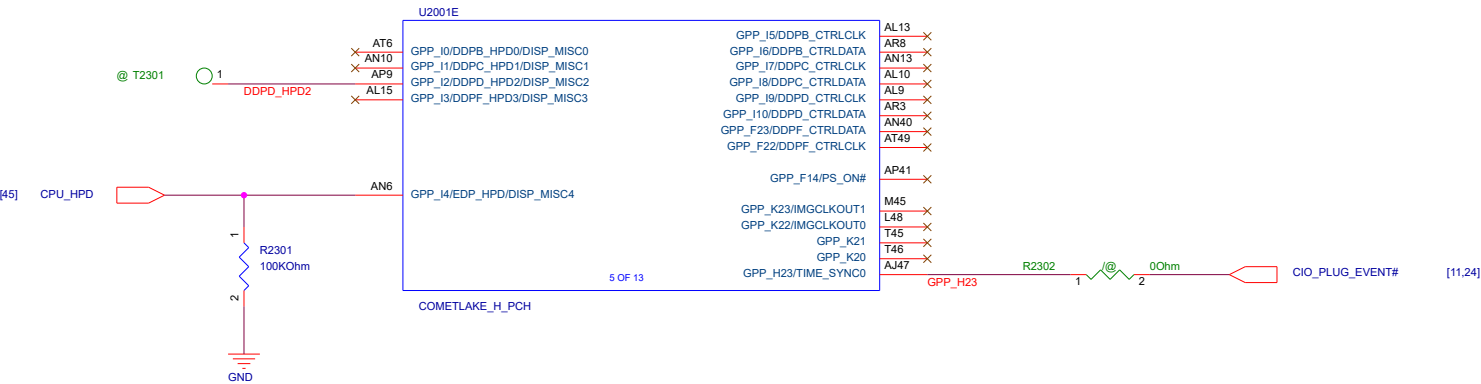
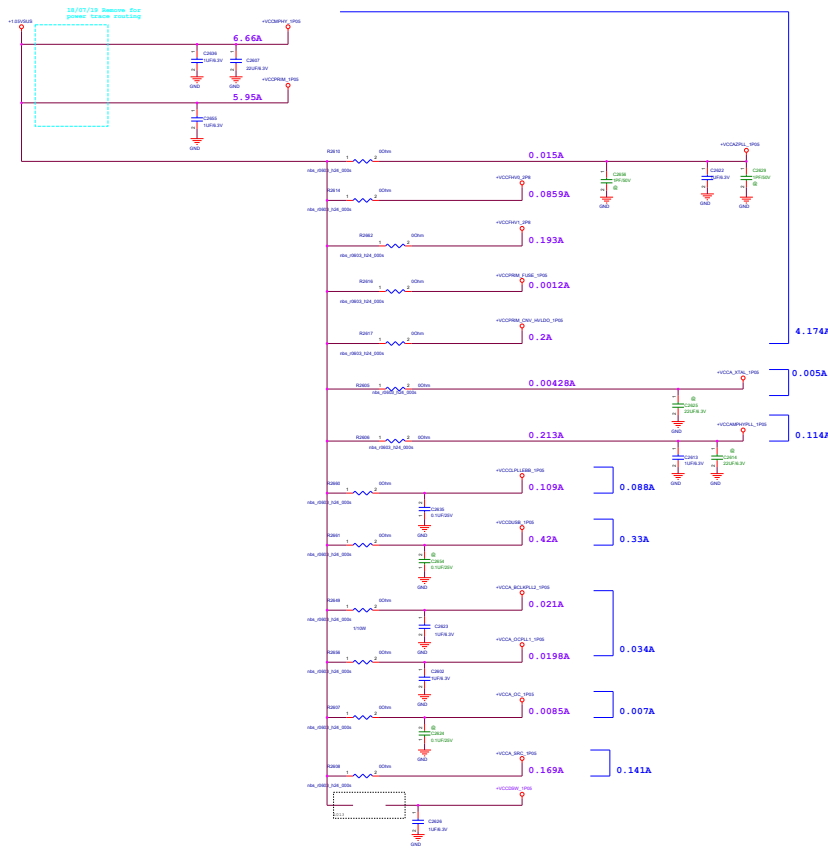
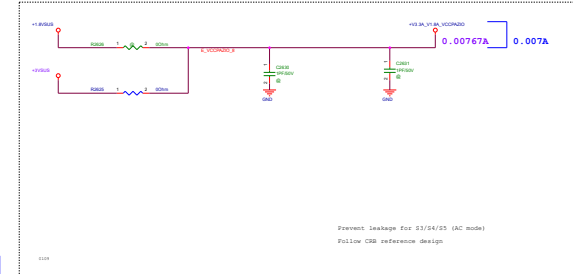
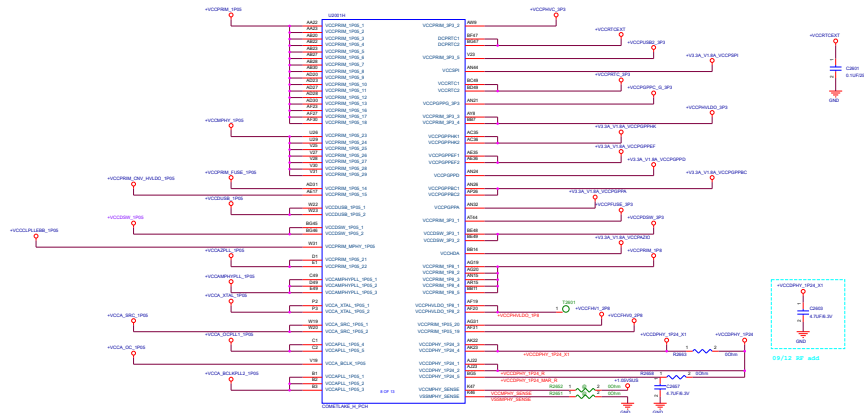
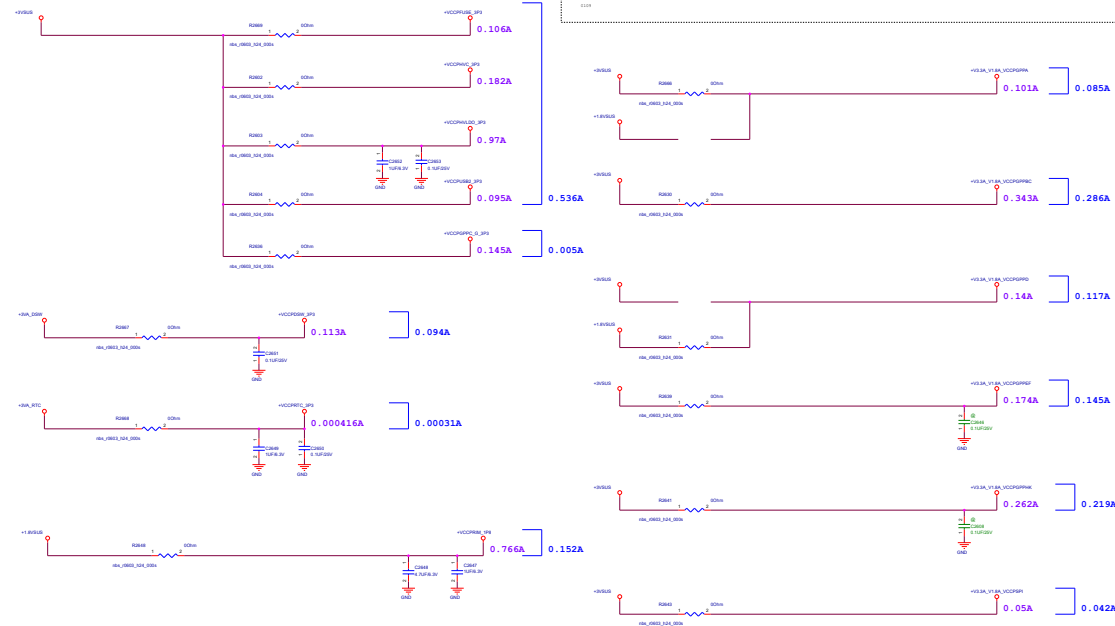
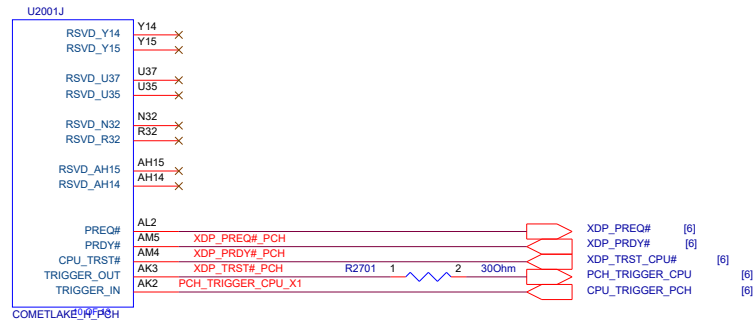
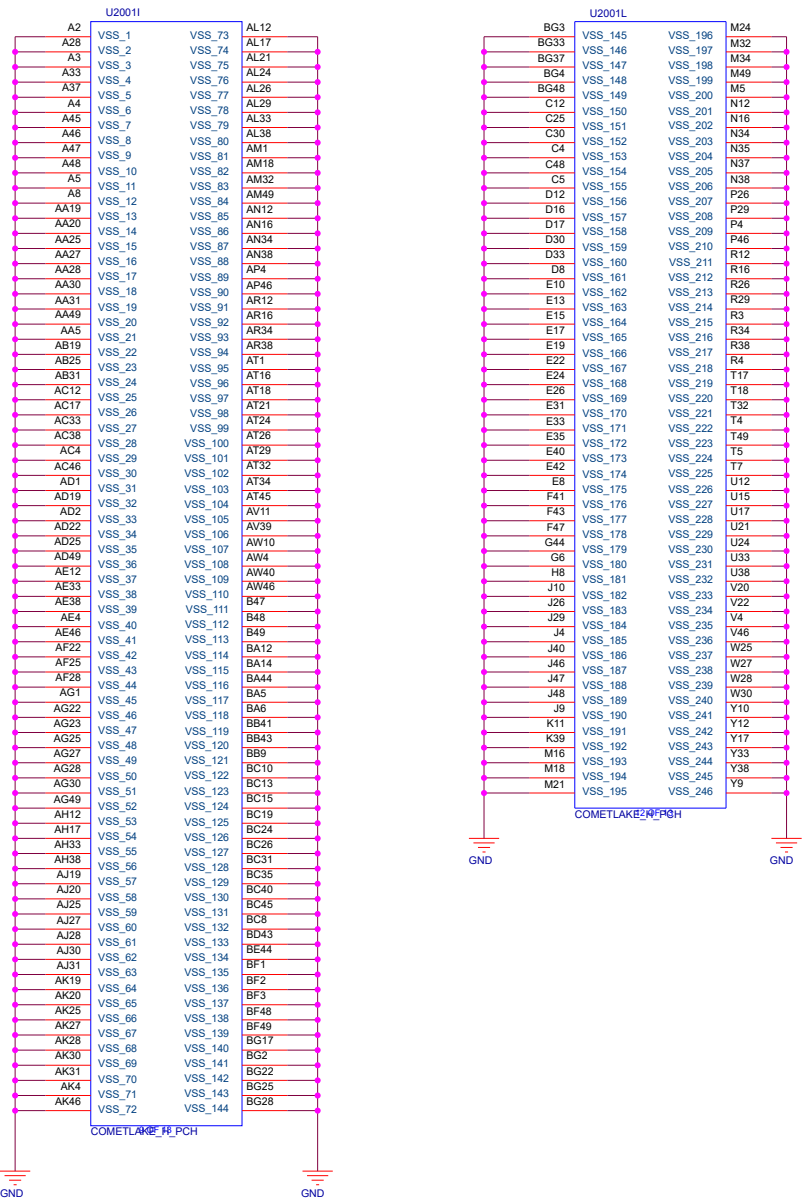


Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPWLDO_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPWLDO_1P8 ball in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_IP3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.

Purple reference CRB
Blue reference EDS



XDP_PREQ# [6]
XDP_PRDY# [6]
XDP_TRST_CPU# [6]
PCH_TRIGGER_CPU [6]
CPU_TRIGGER_PCH [6]



Project Name
GX701

Rev
1.0

Title : PCH-CPT(8), POWER,GND

Size
B Dept.: ASUSTek COMPUTER Engineer: EE

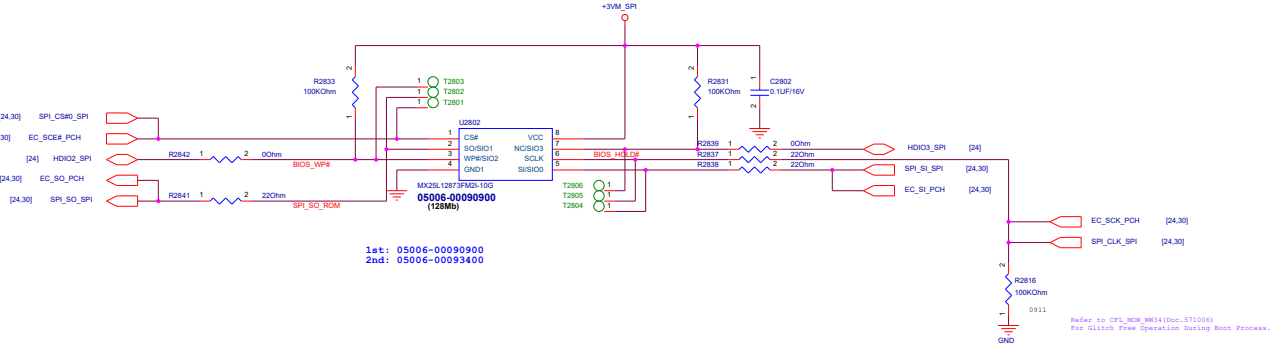
Date: Wednesday, February 12, 2020 Sheet 27 of 103

SPI Power



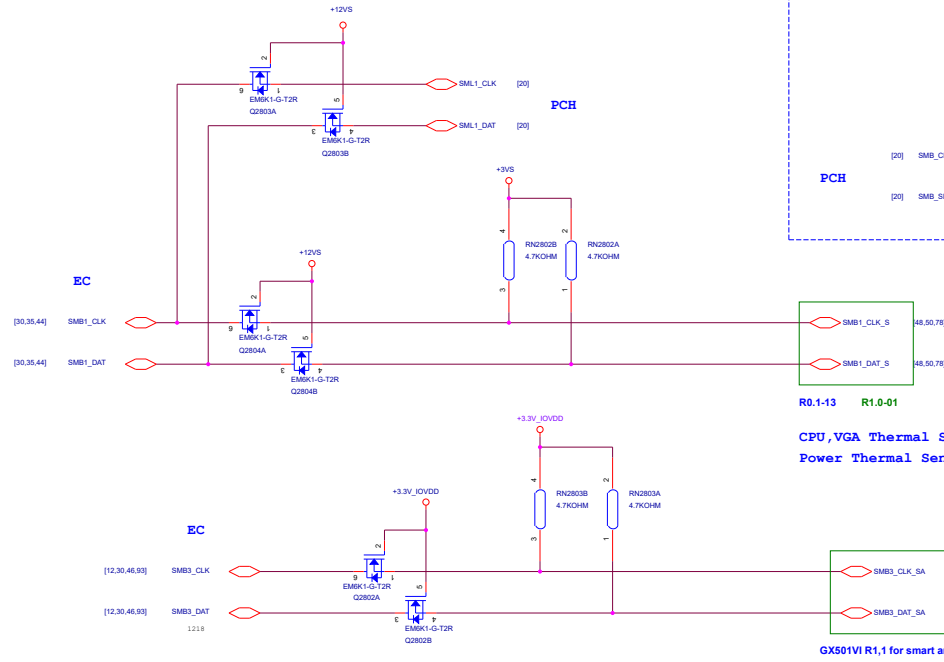
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873PM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

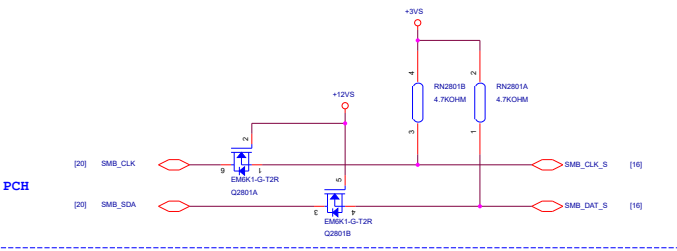


Main Board

System Management Interface

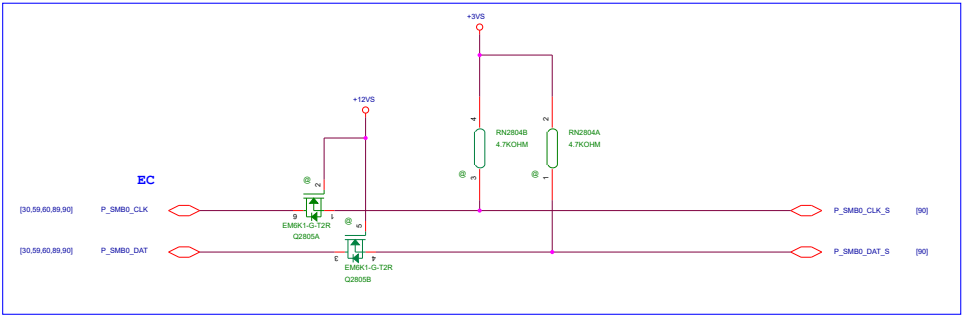



SMBus Interface



R0.1-13 R1.0-01
CPU,VGA Thermal Sensor
Power Thermal Sensor

GX501VI R1,1 for smart amp



		Project Name GX701		Rev 1.0
Title : PCH-XDP				
Size A	Dept.: ASUSTeK COMPUTER		Engineer: EE	
Date: Wednesday, February 12, 2020			Sheet 29	of 103





Project Name

GX701

Rev

1.0

Title : LAN RTL8111GUX-CG


Size

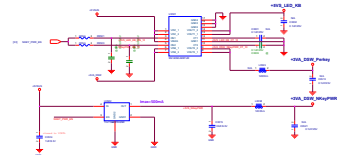
B

Dept.: ASUSTeK COMPUTER INC. NB1 **Engineer:** EE

Date: Wednesday, February 12, 2020

Sheet 33 of 103

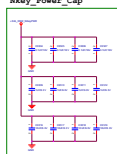
		Project Name	Rev
		GX701	1.0
Title : LAN RJ45 Conn.			
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: EE		
B			
Date: Wednesday, February 12, 2020	Sheet	34	of 103



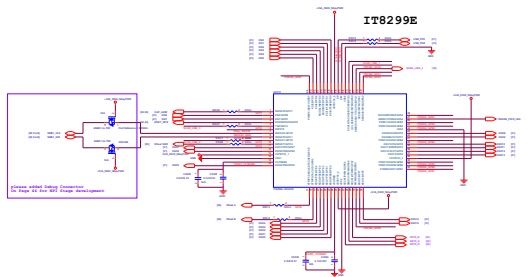
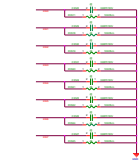
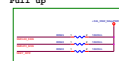
For EC Reset N_Key



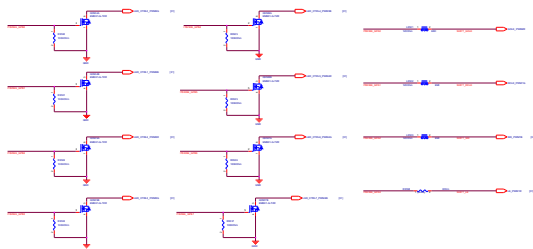
Nkey_Power_Cap



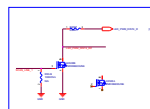
Pull up



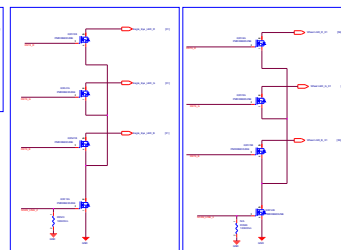
KB RGB LED



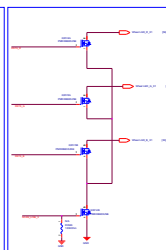
TP LED

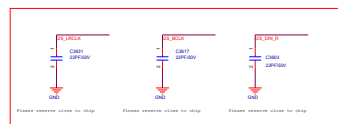
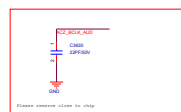
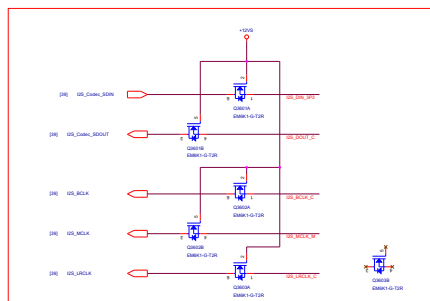
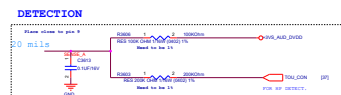
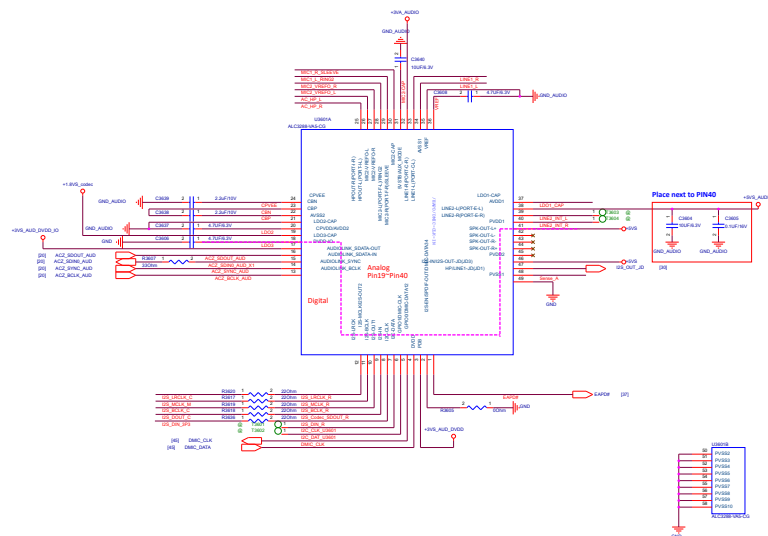
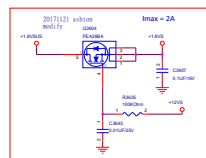
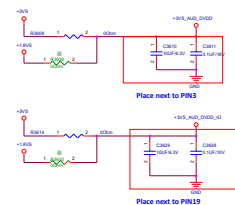
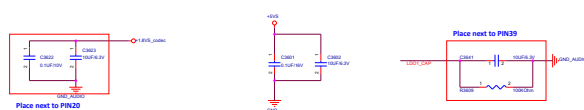
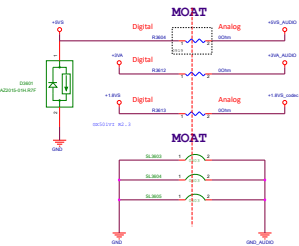


Eagle Eye LED

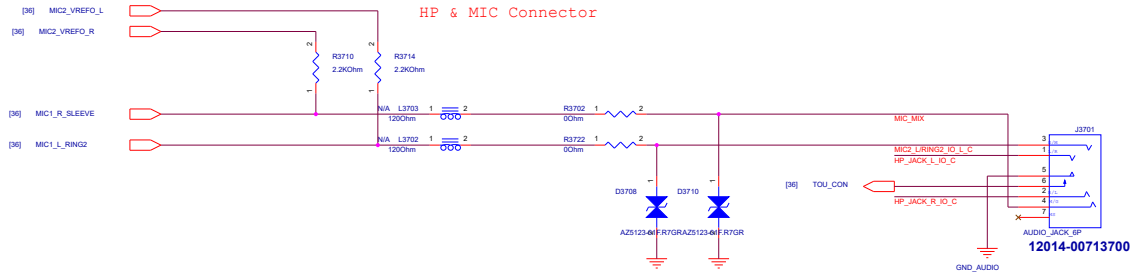
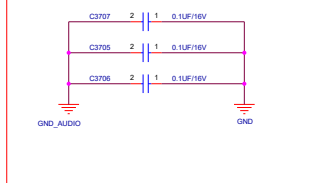


Wheel LED

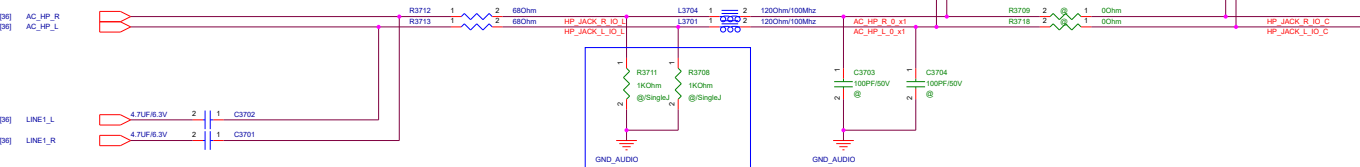
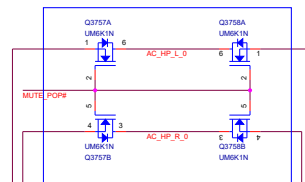




A_GND / GND



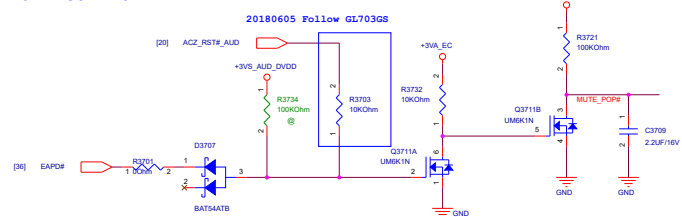
2016.09.06 Add DESPOP solution



2015.04.14 3 pole mic design and VB2 Reserve

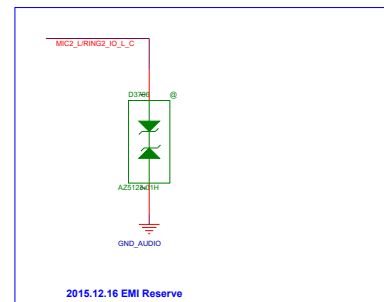
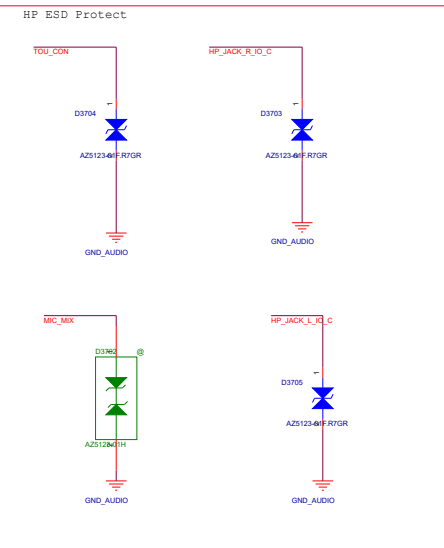
2015.08.07 Realtek Suggest

MUTE CONTROL

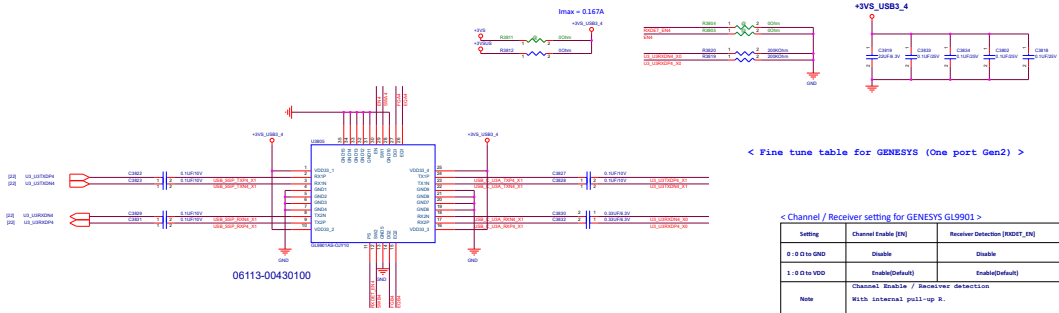


2017.03.23 AMP Change Remove

MUTE CONTROL new solution for 1.8V HDA BUG 0318



teknisi-indonesia



< Fine tune table for GENESYS (One port Gen2) >

< Channel / Receiver setting for GENESYS GL9901 >		
Setting	Channel Enable [FN]	Receiver Detection [RxDIT_FN]
0 : 0 Ohm to GND	Disable	Disable
1 : 0 Ohm to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal pull-up R.	

< EQ table for GENESYS GL9901 >

EQ[A-R]	@2.5Gbps(40)	@5Gbps(40)
0 : 0 Ohm to GND	6.3	10.1
R : Resist to GND	2.2	4.4
F : Leave Open	4.1(Default)	7.1(Default)
1 : 0 Ohm to VDD	7.5	12.5

Note : 0.000000

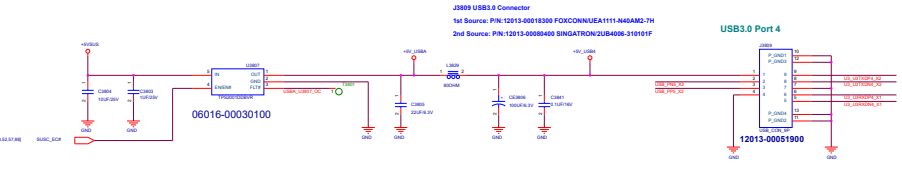
< FG table for GENESYS GL9901 >

FG[A-R]	DC Gain [dB]
0 : 0 Ohm to GND	-2.0
R : Resist to GND	-0.5
F : Leave Open	0.5 (Default)
1 : 0 Ohm to VDD	+2.0

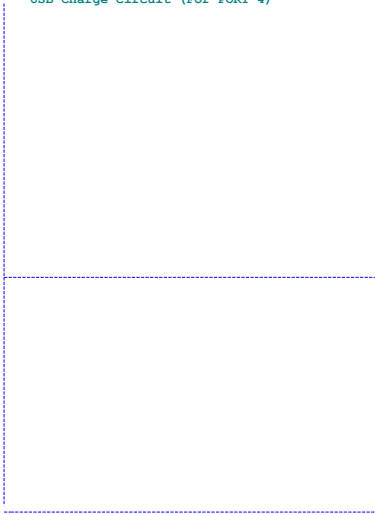
< SW table for GENESYS GL9901 >

SW[A-R]	Output Linear Swing [mV]
0 : 0 Ohm to GND	800
R : Resist to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ohm to VDD	1200

USB3.0_PORT4

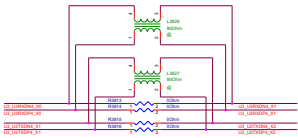


USB Charge Circuit (For PORT 4)

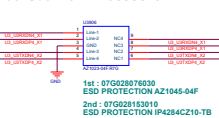


USB3.0 Pin define	
1-	VBUS-
2-	D-
3-	D+
4-	GND-
5-	RX-
6-	RX+
7-	GND-
8-	TX-
9-	TX+

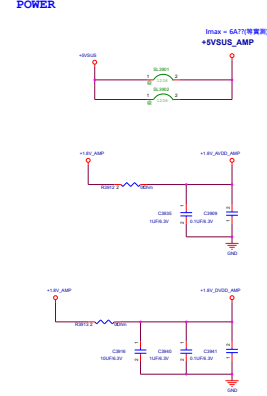
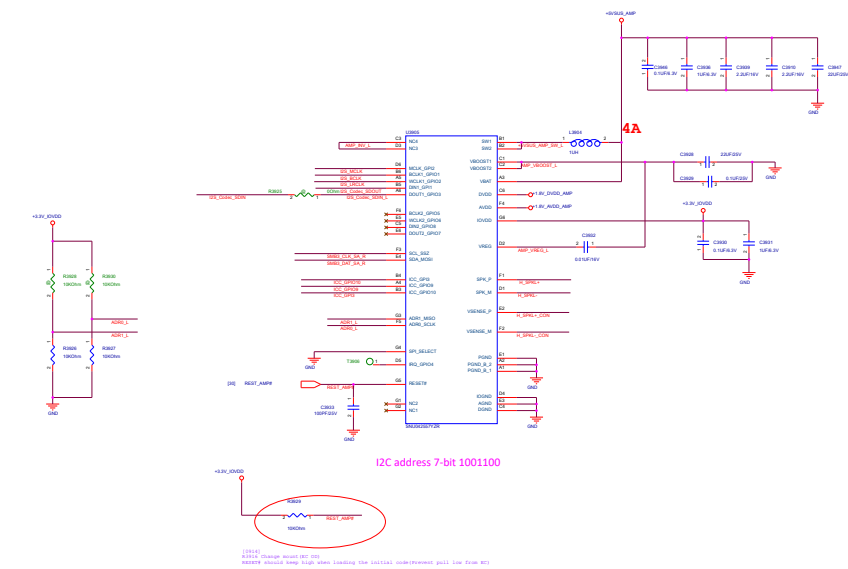
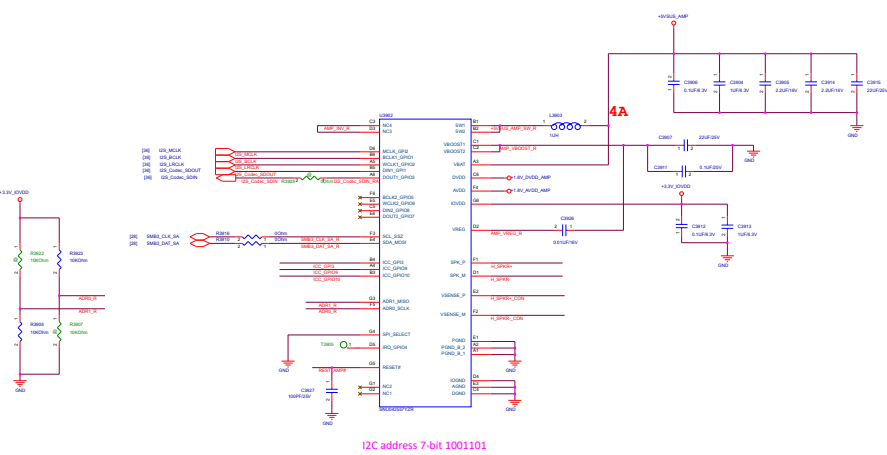
USB3.0_PORT4



USB3.0 ESD-Protection



D1882 ESD Diode
1st Source: PIN:07024-00200200 AMAZING/AZC09-645PRTG
2nd Source: PIN:07024-0070000 NXP/PUSB2K40



11.2 Power Supply Sequencing

The following power sequence should be followed for power up and power down. If the recommended sequence is not followed there can be large current in device due to faults in level shifters and diodes becoming forward biased. The T_{avg} between power supplies should be large enough for the power rails to settle.

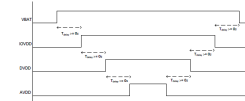
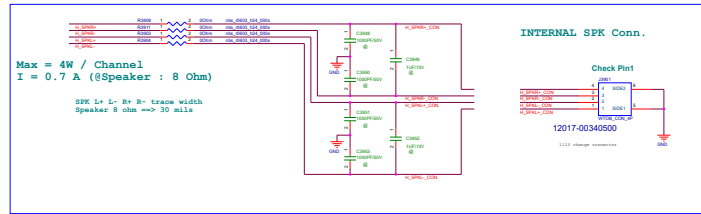


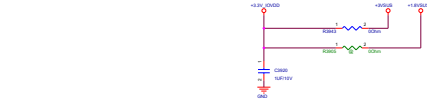
Figure 40. Power Supply Sequence for Power-Up and Power-Down

When the supplies have settled, the RESET terminal can be set HIGH to operate the device. Additionally the RESET pin can be tied to IOVDD and the external DVDD_POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100µs to allow the OTP to load. The above sequence should be completed before any IC operation.



GX701LX 删除预留+1.8V_AMP的LDO线路 2019.07.03

GX701LX 删除预留+3V_AMP的LDO线路 2019.07.03

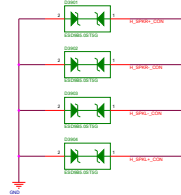


11.1 Power Supplies

The TAS2555 requires four power supplies:


- Boost Input (terminal: VBAT)
 - Voltage: 2.9 V to 5.5 V
 - Max Current: 5 A for ILIM = 3.0 A (default)
- Analog Supply (terminal: AVDD)
 - Voltage: 1.65 V to 1.95 V
 - Max Current: 30 mA
- Digital Supply (terminal: DVDD)
 - Voltage: 1.65 V to 1.95 V
 - Max Current: TBD mA
- Digital I/O Supply (terminal: IOVDD)
 - Voltage: 1.62 V to 3.6 V
 - Max Current: 5 mA

INTERNAL SPK Conn.



Copyright 2019

<Variant Name>

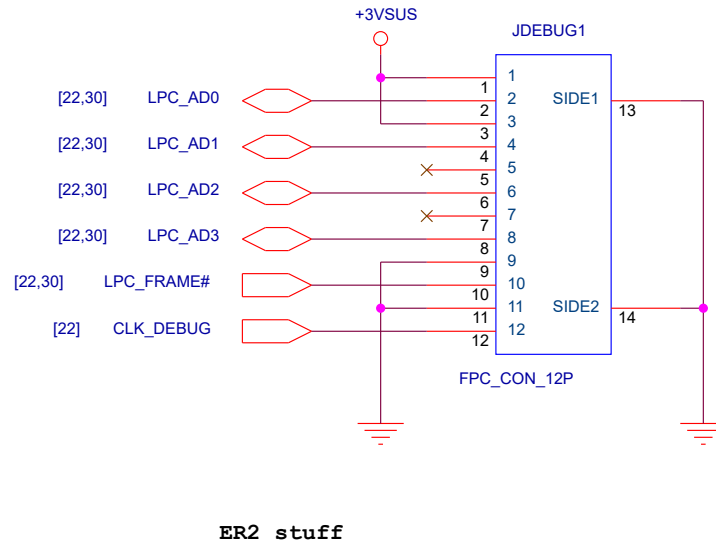
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ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 41 of 103	

<Variant Name>

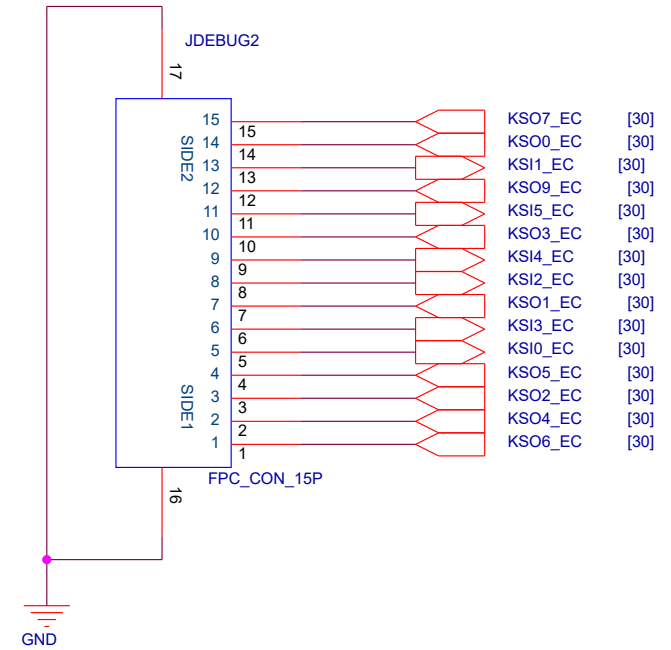
		Title : HDMI_DP_Switch	
ASUSTeK COMPUTER INC. NBI		Engineer: EE	
Size	Project Name		Rev
C	GX701		1.0
Date:	Wednesday, February 12, 2020	Sheet	42 of 103

2017/11/10

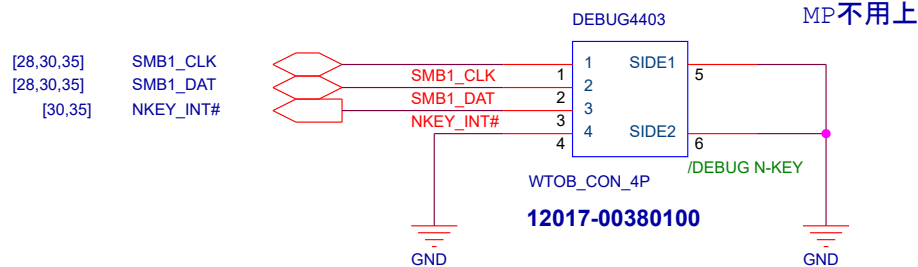
LPC Debug Port




2017/11/10



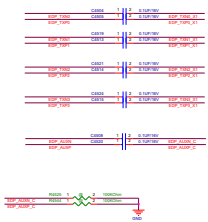
N-KEY Debug Connector



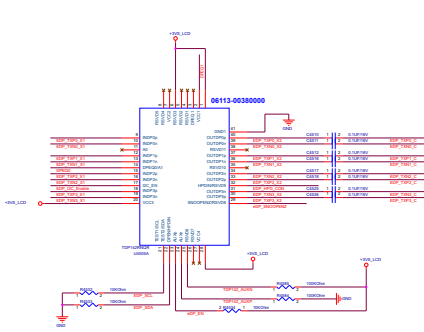
<Variant Name>

		Title : DEBUG_LPC	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020	Sheet 44 of 103		

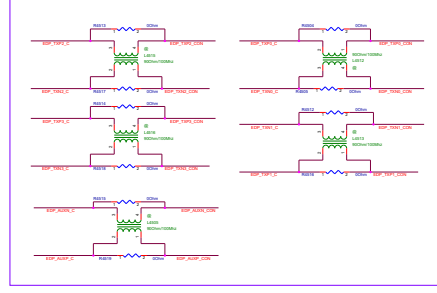
eDP from CPU



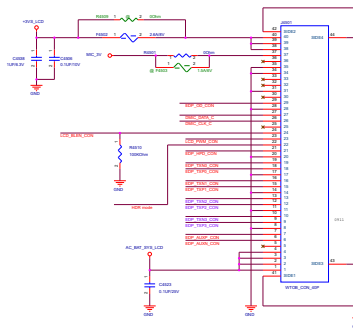
EDP1.4 Re-driver



For eDP EMI



eDP Panel Conn.



MIC

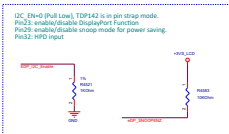
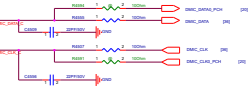
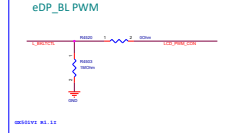
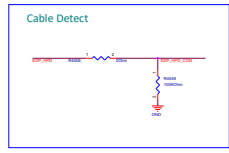
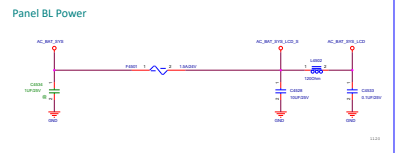


Table 1. 4-Level Control Pin Settings	
LEVEL	SETTINGS
0	Option 1: The 1 kΩ 5% to GND Option 2: The directly to GND
B	The 20 kΩ 5% to GND Fixed above on cases
F	Option 1: The 1 kΩ 5% to V _{DD} Option 2: The directly to V _{DD}
E	



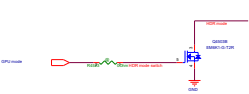
MIC module



OD Control



HDR mode Control

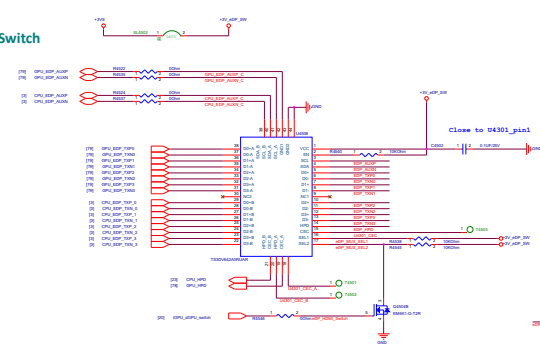


Default: Floating (OD disable)
Active: 1 (OD enable)

Optimize Mode(HDR400 ON, -Gsync OFF)
Discrete Mode(HDR400 OFF, -Gsync ON)

ODP_ODP_ODP_ODP	ODP_ODP_ODP	ODP_ODP_ODP
0	Forcing (OD enable)	Optimize
B	Low	Discrete

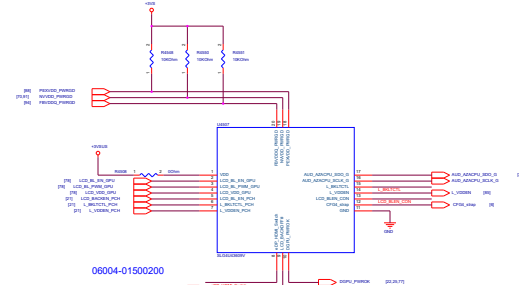
eDP Switch



ODP_ODP_ODP	ODP_ODP_ODP	ODP_ODP_ODP
0	Forcing (OD enable)	Optimize
B	Low	Discrete

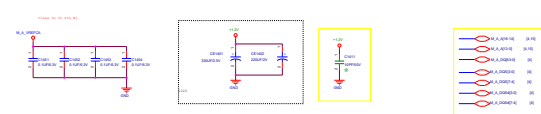
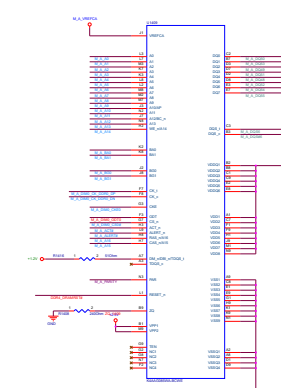
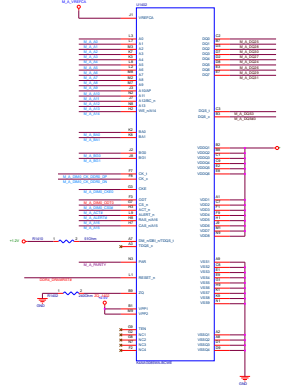
ODP_ODP_ODP	ODP_ODP_ODP	ODP_ODP_ODP
0	Forcing (OD enable)	Optimize
B	Low	Discrete

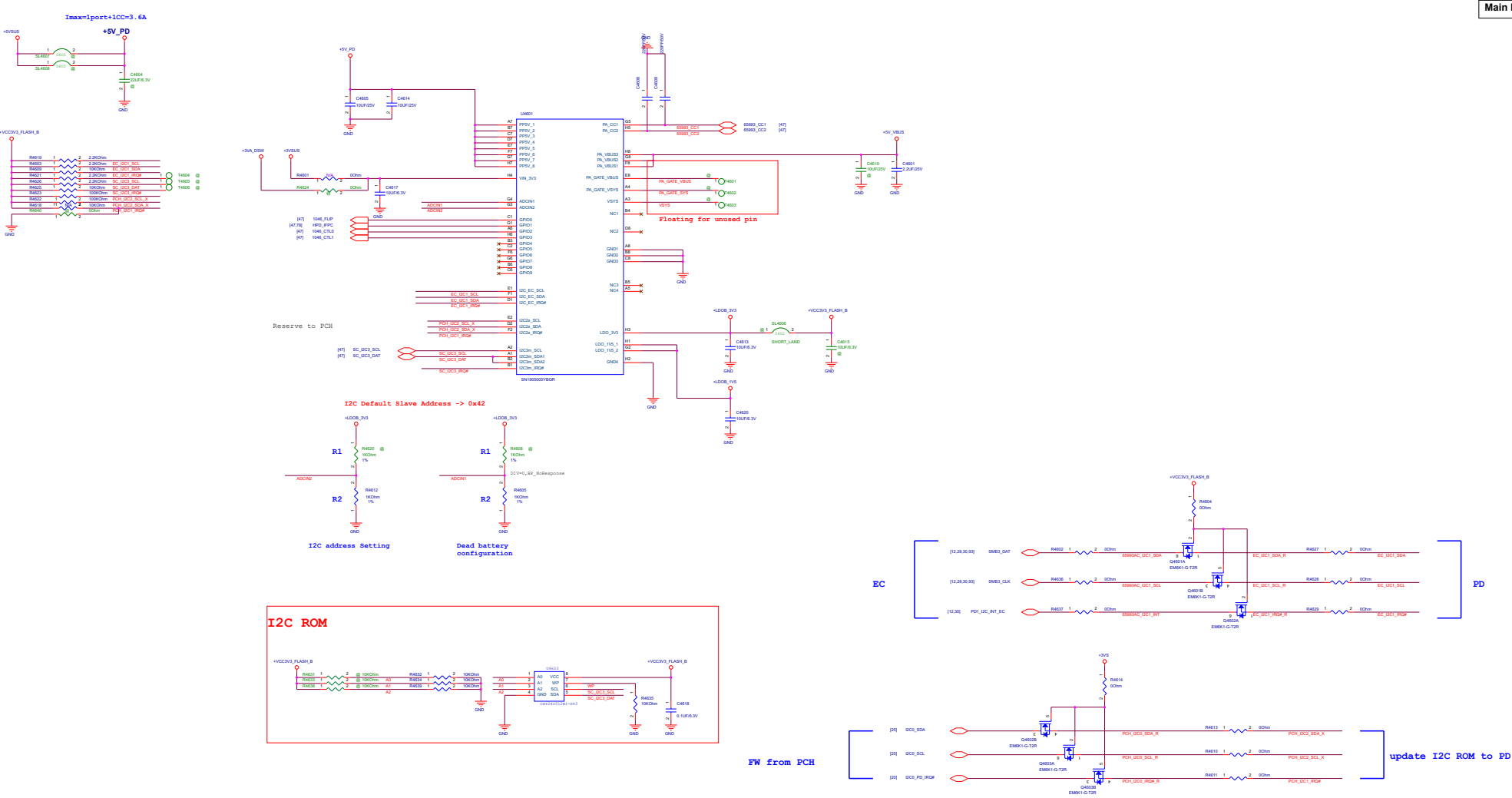
BL_EN/BL_PWM/L_VDDEN SWITCH IC(Switchable Use)

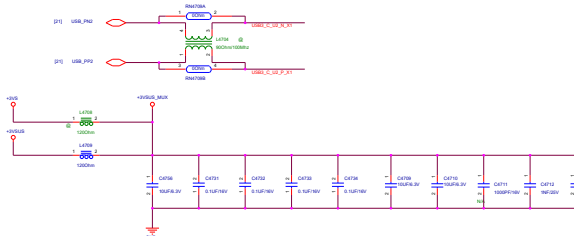
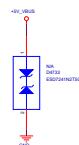
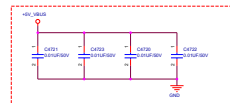


ODP_ODP_ODP	ODP_ODP_ODP	ODP_ODP_ODP
0	Forcing (OD enable)	Optimize
B	Low	Discrete

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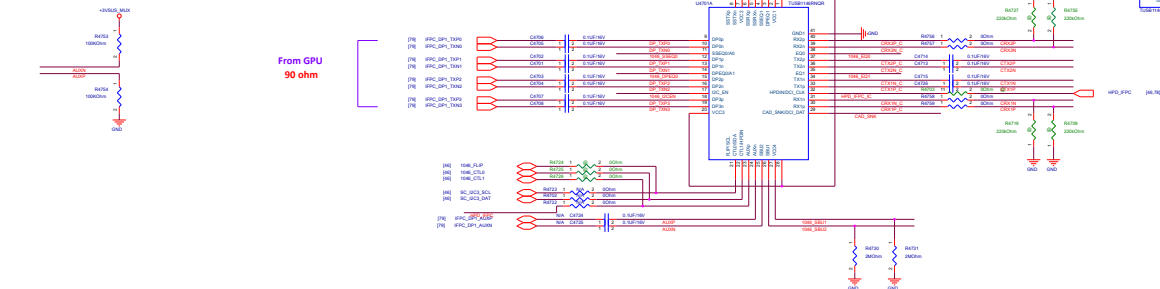




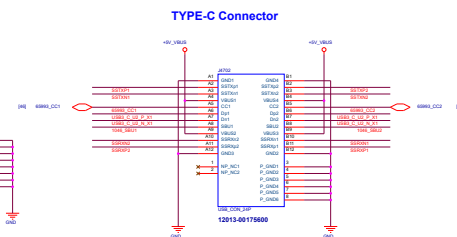
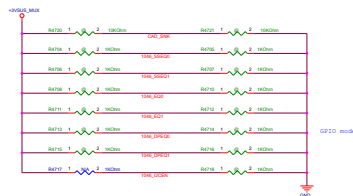
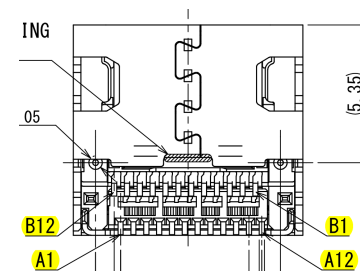
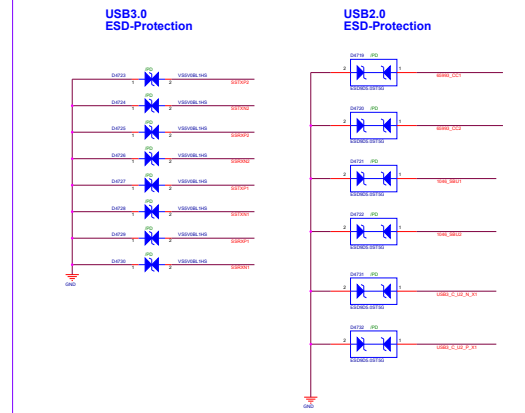
NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

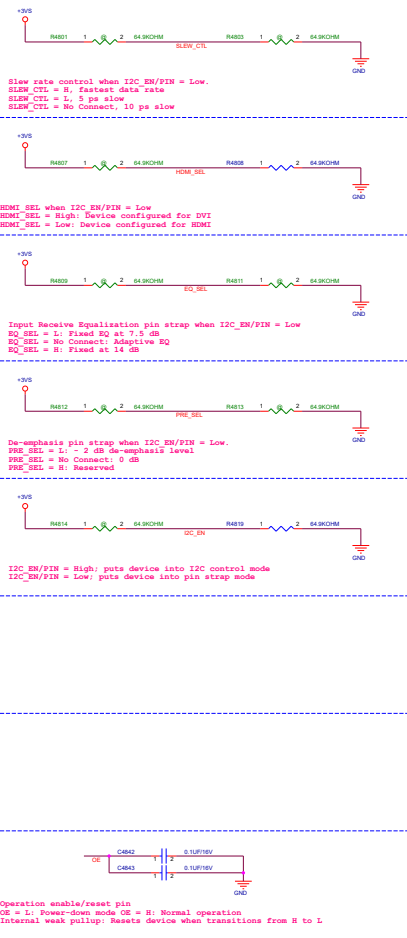
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V _{BUS}	CC1	D+	D-	SBU1	V _{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V _{BUS}	SBU2	D-	D+	CC2	V _{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

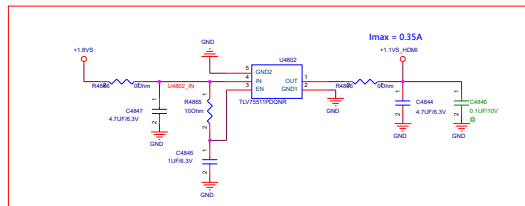


CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB14646-DCI CONFIGURATION	VEESA DisplayPort ALT MODE DFP_0 CONFIGURATION
L	L	L	Power Down	—
L	H	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
H	H	H	One Port USB 3.1 - With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP - With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP, No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP, With Flip	D and F

USB
ESD-Protection



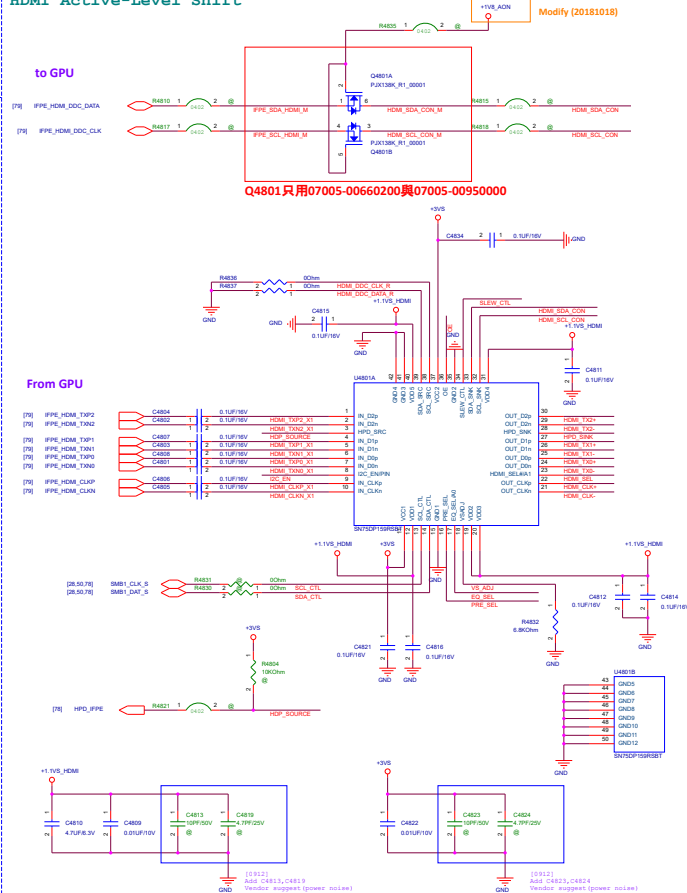
HDMI LDO 1.1VS



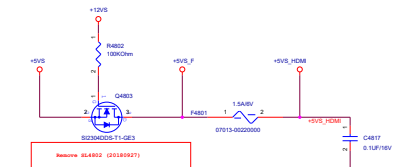
2019/07/02 删除预留的LDO solution



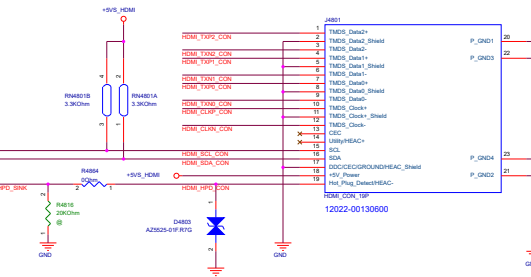
HDMI Active-Level Shift



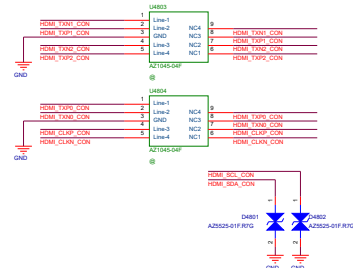
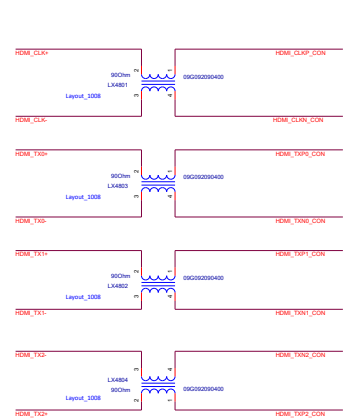
HDMI PWR_+5VS_HDMI



HDMI Conn.



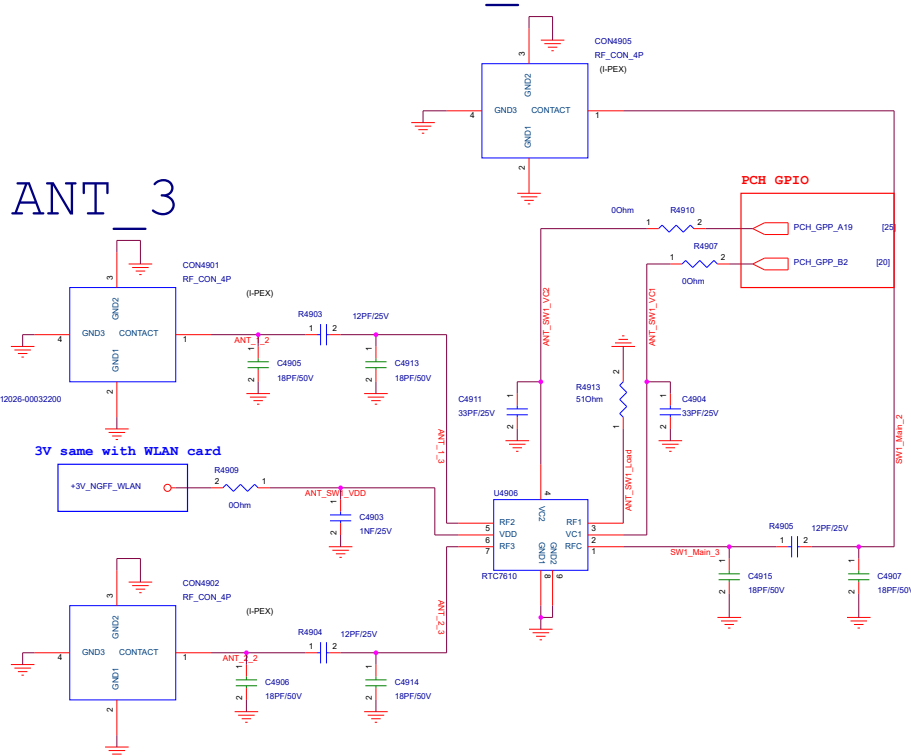
HDMI EMI



Module_AUX

Module_MAIN

ANT_3

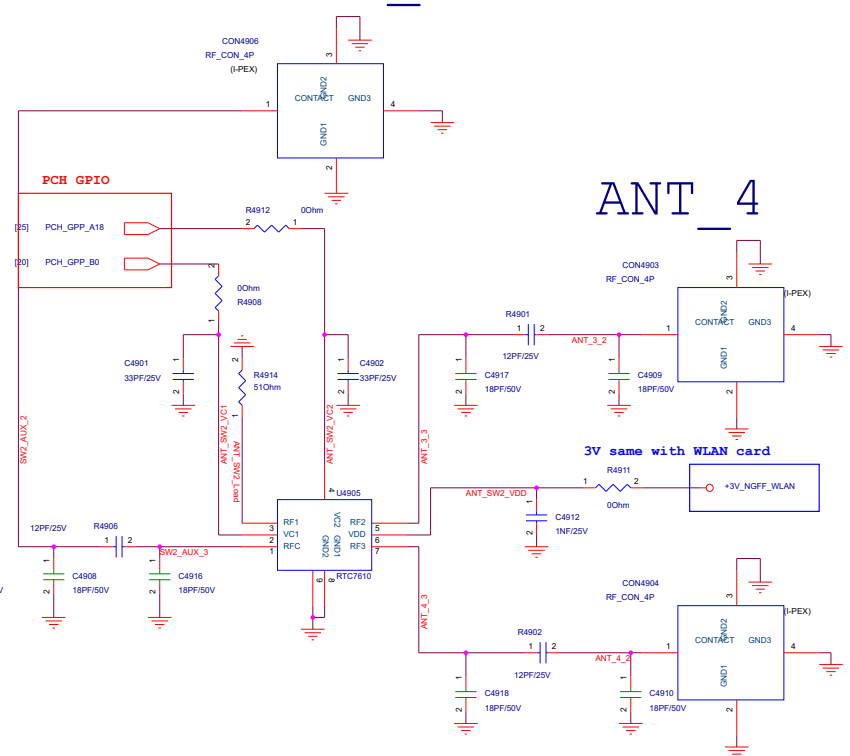


ANT_1

U4906 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

ANT_4



ANT_2

U4905 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

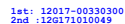
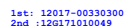
X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

SMBUS1 to EC

Pin function Supply voltage.: 1.62 V to 3.6 V

SMBUS addr=10010000 (90)



SMBUS addr=10010001 (91)



DC FAN Control 2

SMBUS addr=10010010 (92)

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 90	Ground	CPU
1001001 91	V+	VRAM
1001010 92	SDA	GPU
1001011 93	SCL	



Title : TYPE-C USB3.1_R1.5_4

ASUSTeK COMPUTER INC. NB1

Engineer:

Size

Project Name

Rev

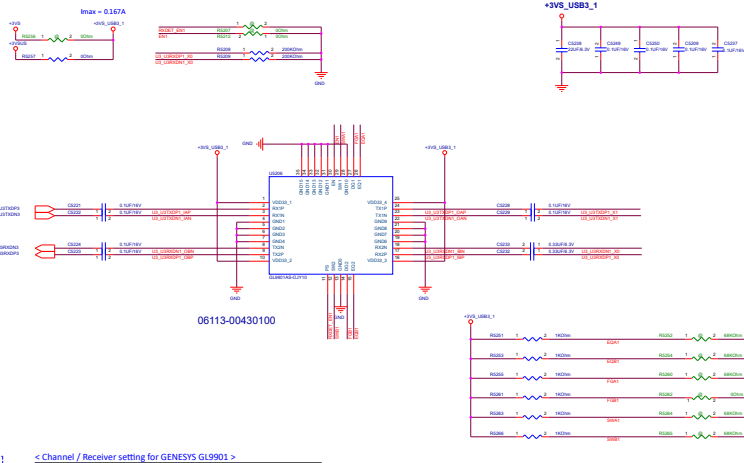
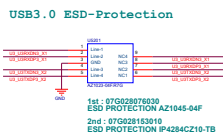
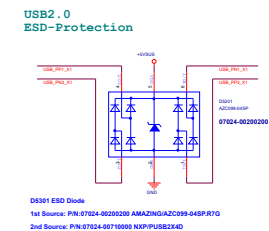
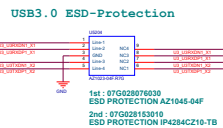
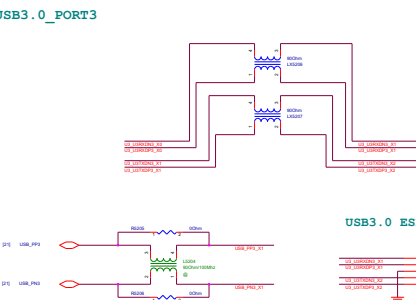
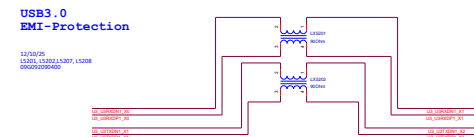
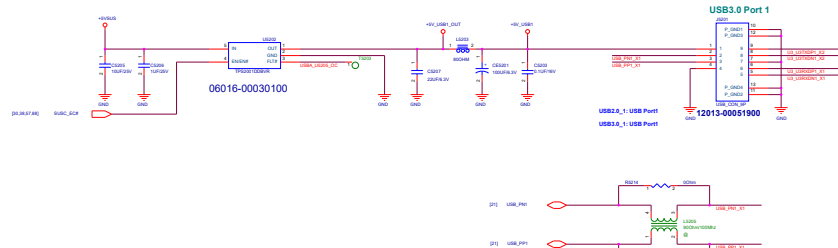
D

GX701

R1.5

Date: Wednesday, February 12, 2020

Sheet 51 of 103



< Channel / Receiver setting for GENESYS GL9901 >

Setting	Channel Enable [FN]	Receiver Detection [RXDET_FN]
0 : 0.0 to GND	Disable	Disable
1 : 0.0 to VDD	Enable(Default)	Enable(Default)

Note: Channel Enable / Receiver detection With internal pull-up R.

< SW table for GENESYS GL9901 >

SW[A]	Output Linear Swing [mV]
0 : 0.0 to GND	800
R: Rest to GND	1200
F: Leave Open	1000 (Default)
1 : 0.0 to VDD	1000

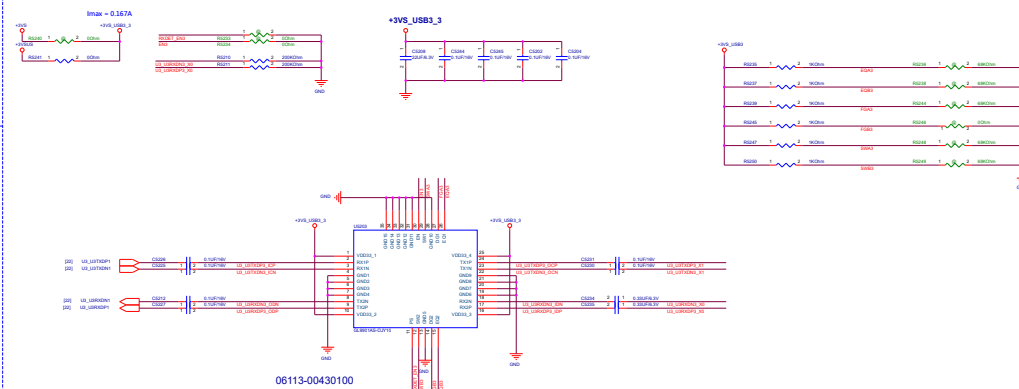
< FG table for GENESYS GL9901 >

FG[A]	DC Gain [dB]
0 : 0.0 to GND	-2.0
R: Rest to GND	-0.5
F: Leave Open	0.5 (Default)
1 : 0.0 to VDD	+2.0

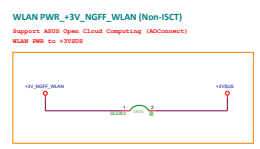
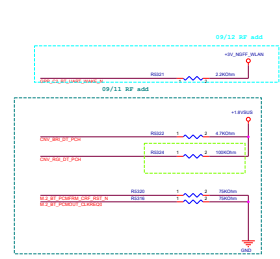
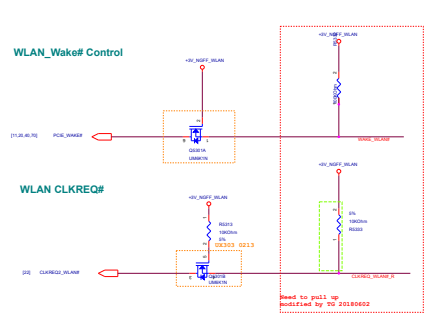
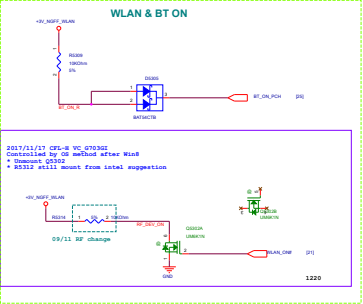
< Fine tune table for GENESYS (One port Gen2) >

EQ[A]	@2.50mV/m	@10mV/m
0 : 0.0 to GND	6.5	10.5
R: Rest to GND	2.2	6.8
F: Leave Open	4.5(Default)	7.5(Default)
1 : 0.0 to VDD	7.0	11.0

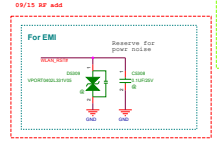
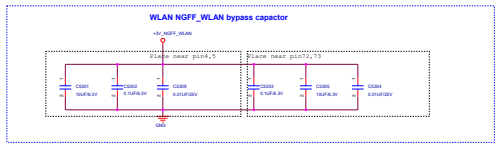
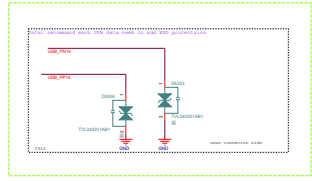
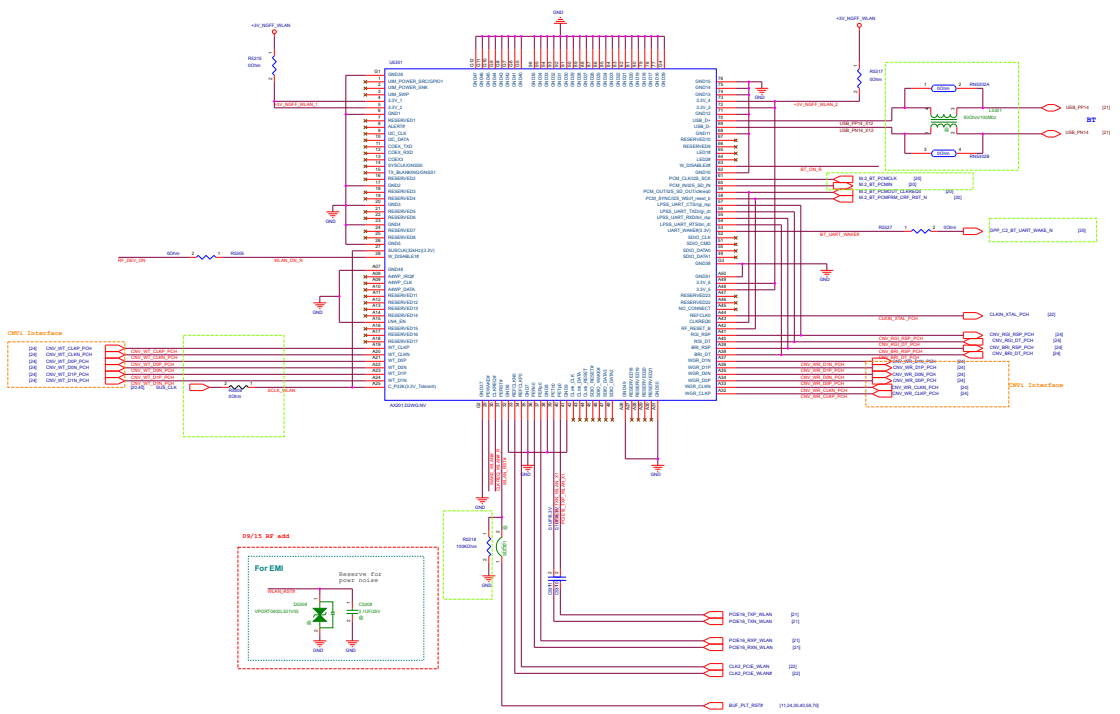
Note: 100mV/m



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SD-1216

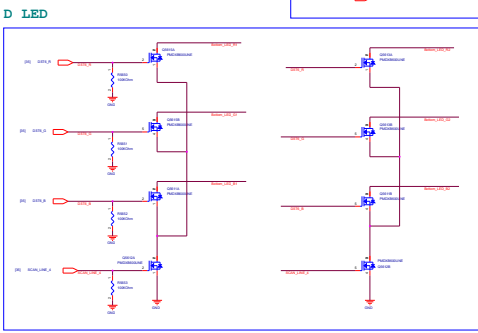
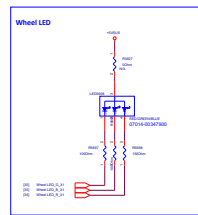
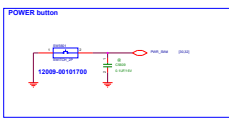
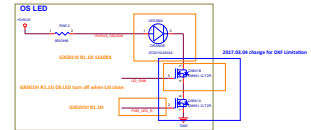
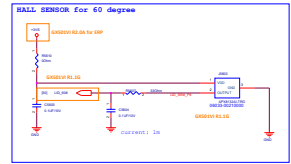
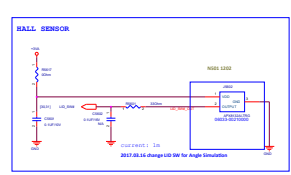
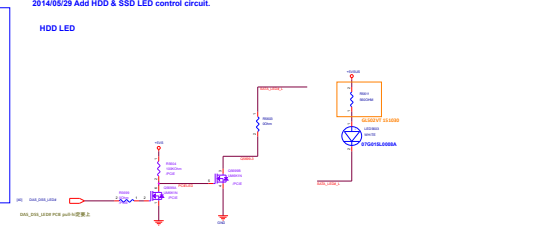
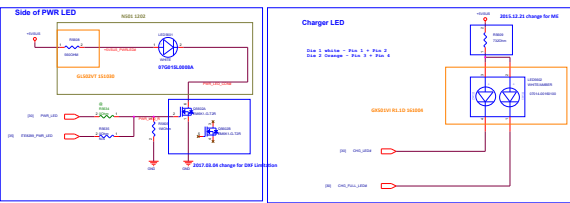


«Variant Name»

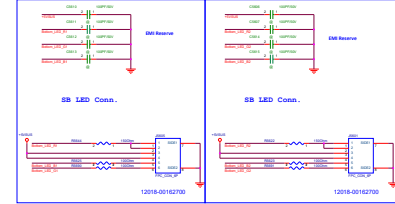
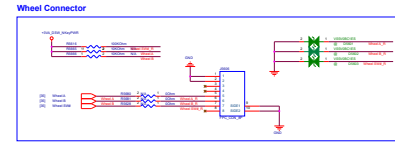
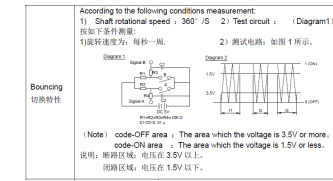
		Title :	USB3_*****
ASUSTeK COMPUTER INC		Engineer:	EE
Size	Project Name	Rev	
Custom	GX701	1.0	
Date:	Wednesday, February 12, 2020	Sheet	54 of 503

<Variant Name>

		Title : IO Con. to MB	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size Custom	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 55 of 103	

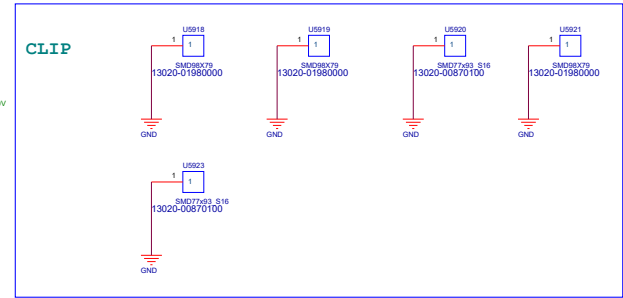
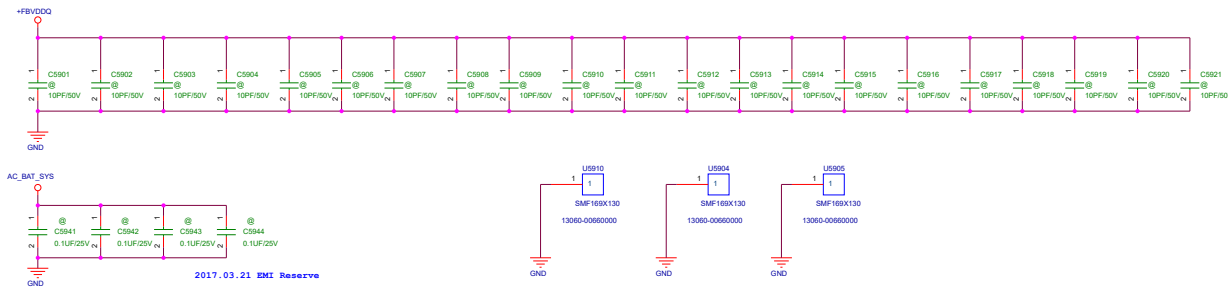


Shift rotational direction 转动的方向	Signal 信号	Output 输出信号
C.W. 顺时针方向	A 1~C 端子线 A 1 Terminal 1~C1	VPP
	B 1~C 端子线 B 1 Terminal 1~C1	ON
C.C.W. 逆时针方向	A 1~C 端子线 A 1 Terminal 1~C1	ON
	B 1~C 端子线 B 1 Terminal 1~C1	ON

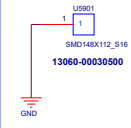


svgexport-53.svg --

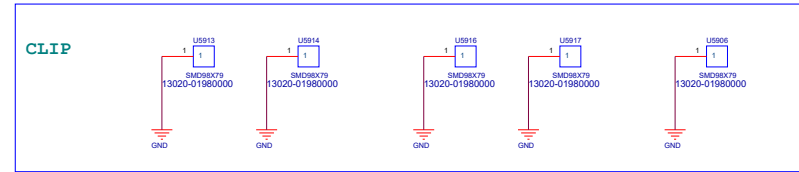
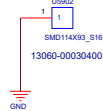
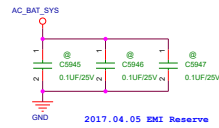
2016/06/08 EMI



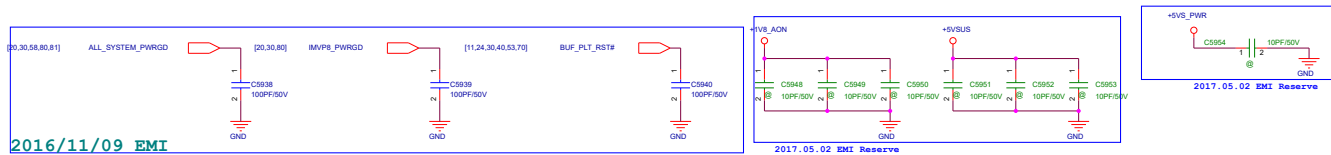
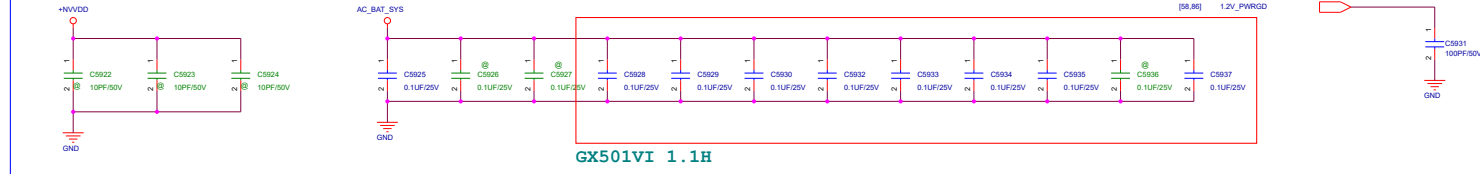
2016/08/05 EMI



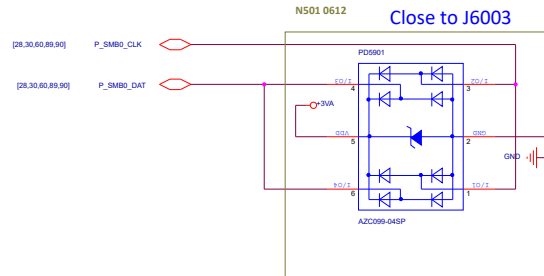
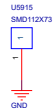
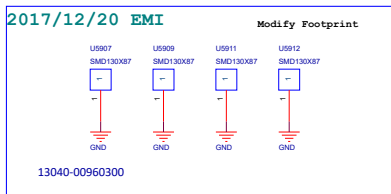
2017/04/05 EMI



2016/07/27 EMI



2016/11/09 EMI

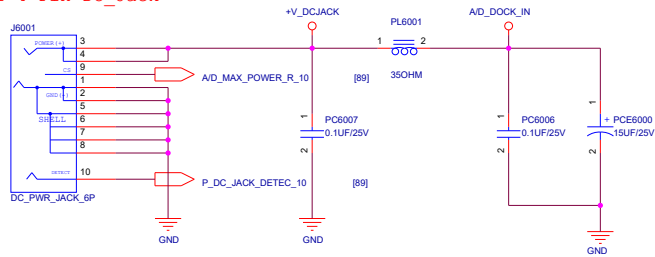


<Variant Name>

DC-IN Connector

DC Jack使用請詢用River_Hsu

New 6 Phi 4 Pin DC_Jack




J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300


Battery Connector




<Variant Name>

		Title : BT_Blueetooth	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 61 of 103	


<Variant Name>

		Title : I/O board(1-1)_CR_RTS5139	
ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 62 of 103	

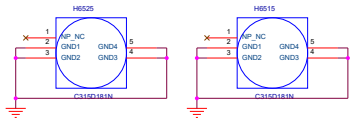
<Variant Name>

		Title : USB Port	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 63 of 103	

<Variant Name>

		Title : I/O board(1-3)_USB	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 64 of 103	

8/4.6



2.2



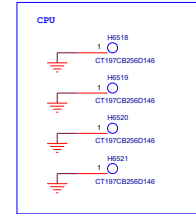
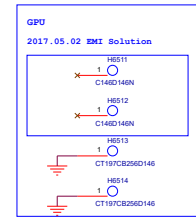
2.5



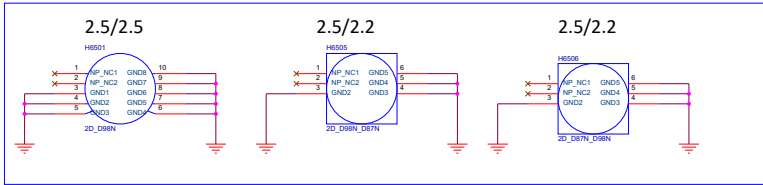
8.5



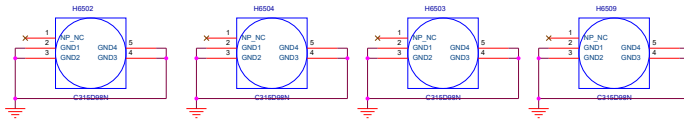
3.2/2.2



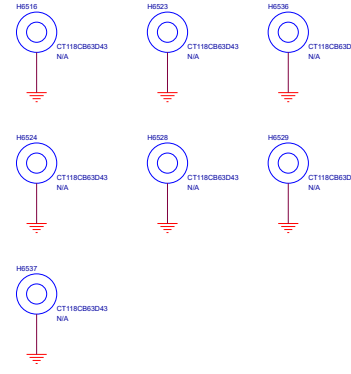
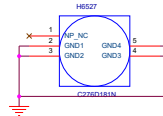
Irregular hole



8/2.5




7/4.6




<Variant Name>


<Variant Name>

		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer:	EE
Size	Project Name		Rev
D	GX701		1.0
Date:	Wednesday, February 12, 2020	Sheet	66 of 103


<Variant Name>

		Title : I/O board FUNC key	
ASUSTeK COMPUTER		Engineer: EE	
Size E	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 67 of 103	

<Variant Name>

		Title : OTH_for test only	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size D	Project Name teknisi-indonesia GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 68 of 103	

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer:	EE
Size	Project Name		Rev
D	GX701		1.0
Date:	Wednesday, February 12, 2020	Sheet	69 of 103

Main Board

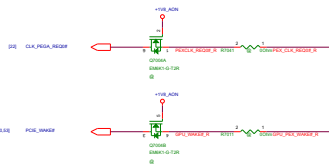


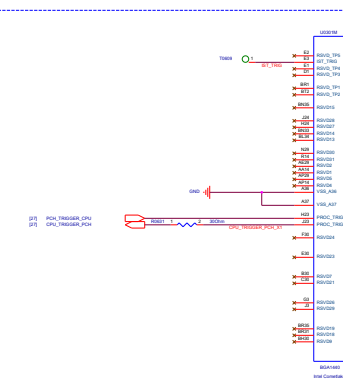
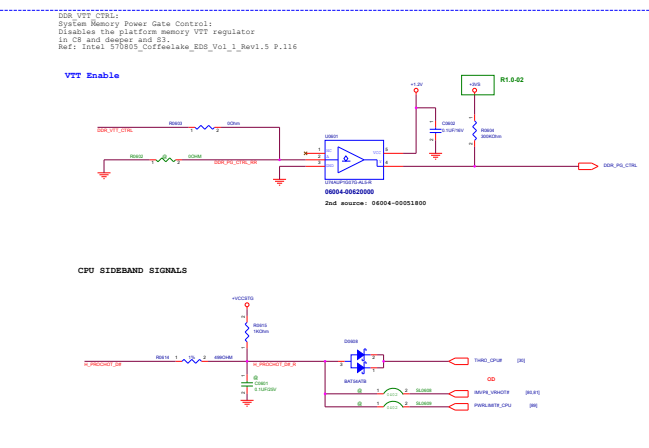
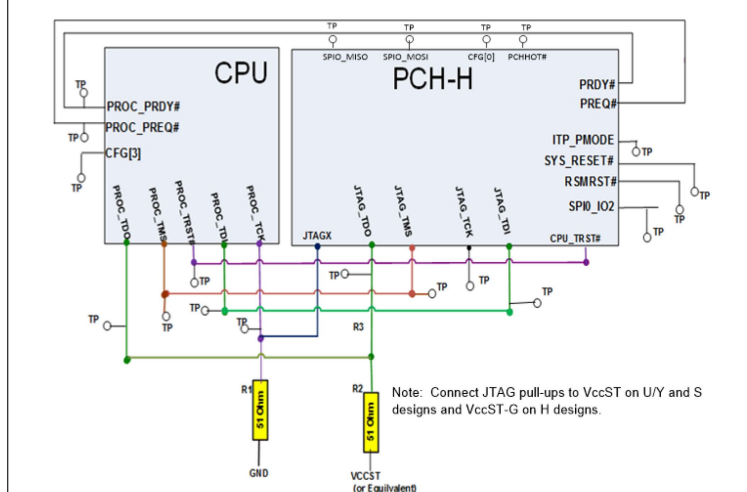
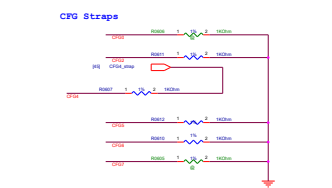
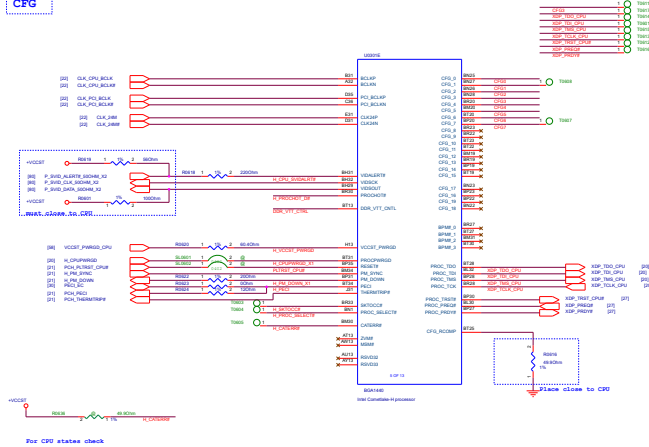
PCH_GPPXB

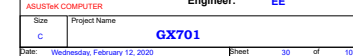


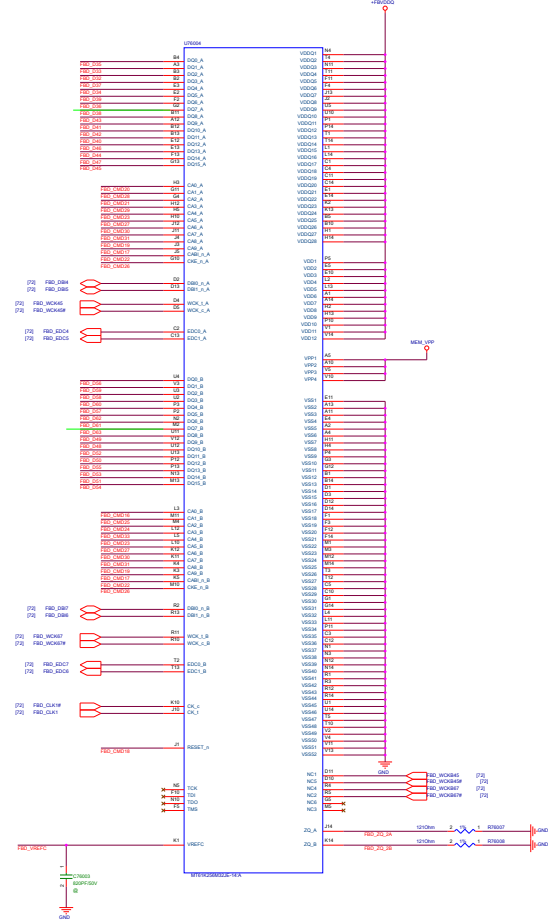
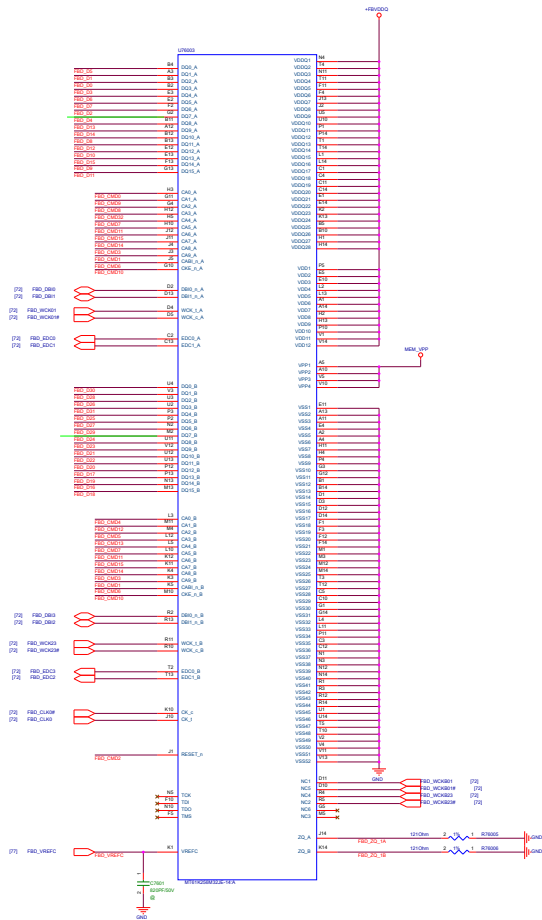
PCN_OPCODE	FUNCTION
R	enter GC OFF
L	exit GC OFF

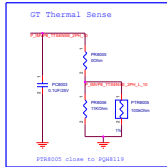
20190327 change CPLD LOGIC SLG4U42939V

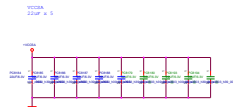
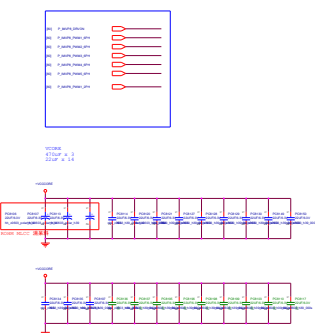
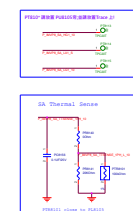
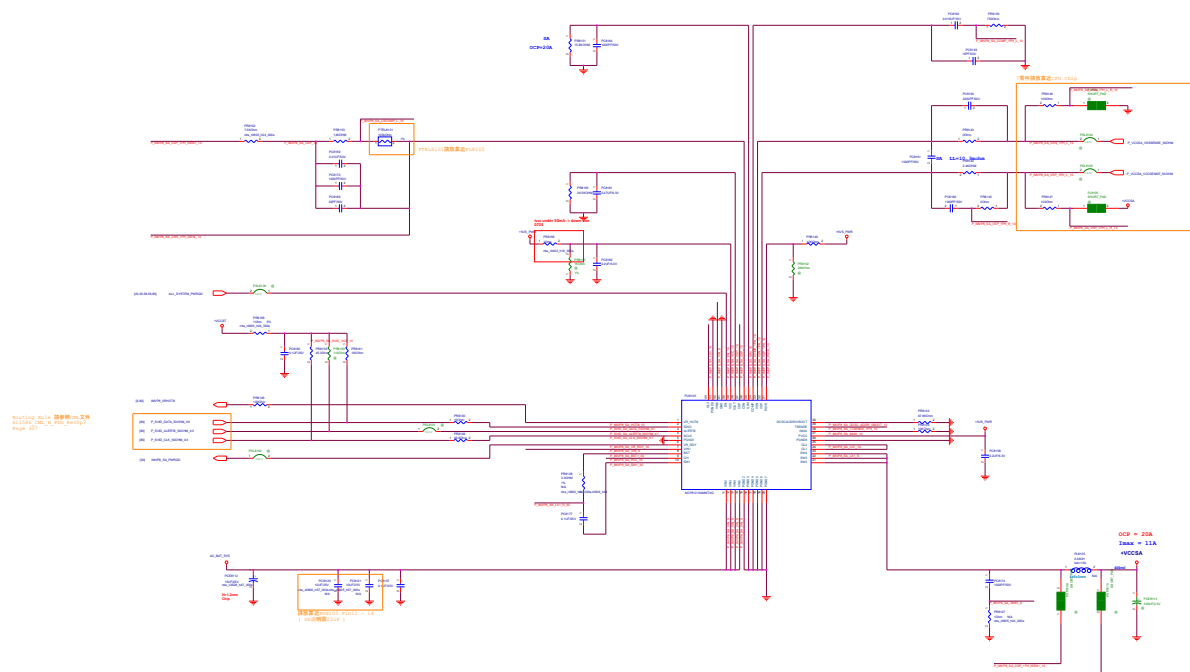
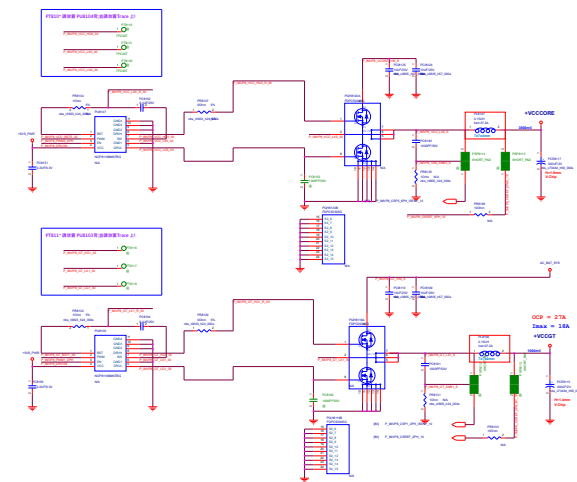
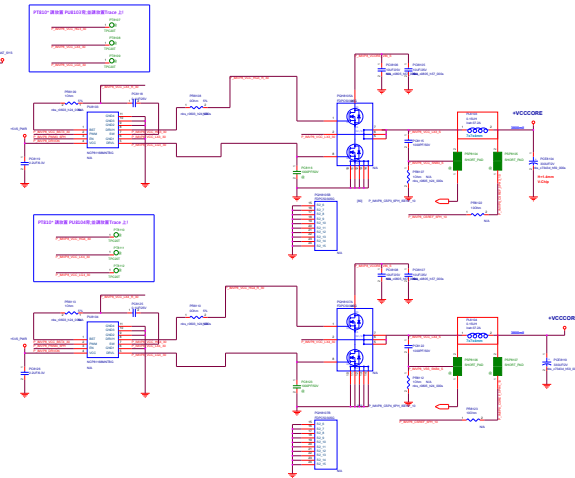
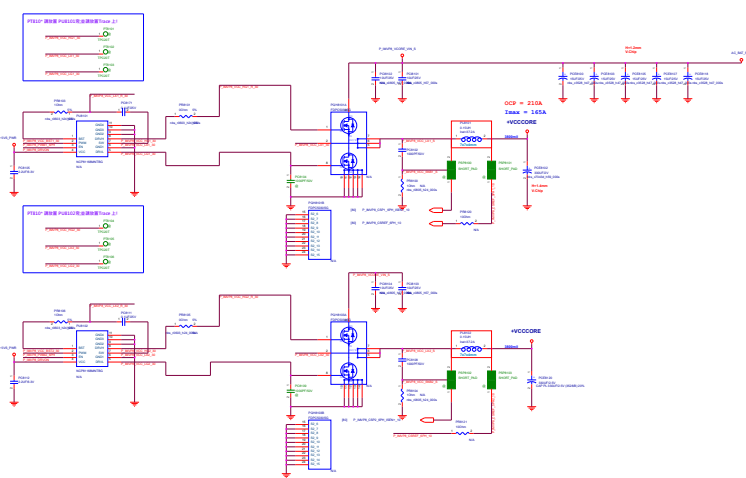




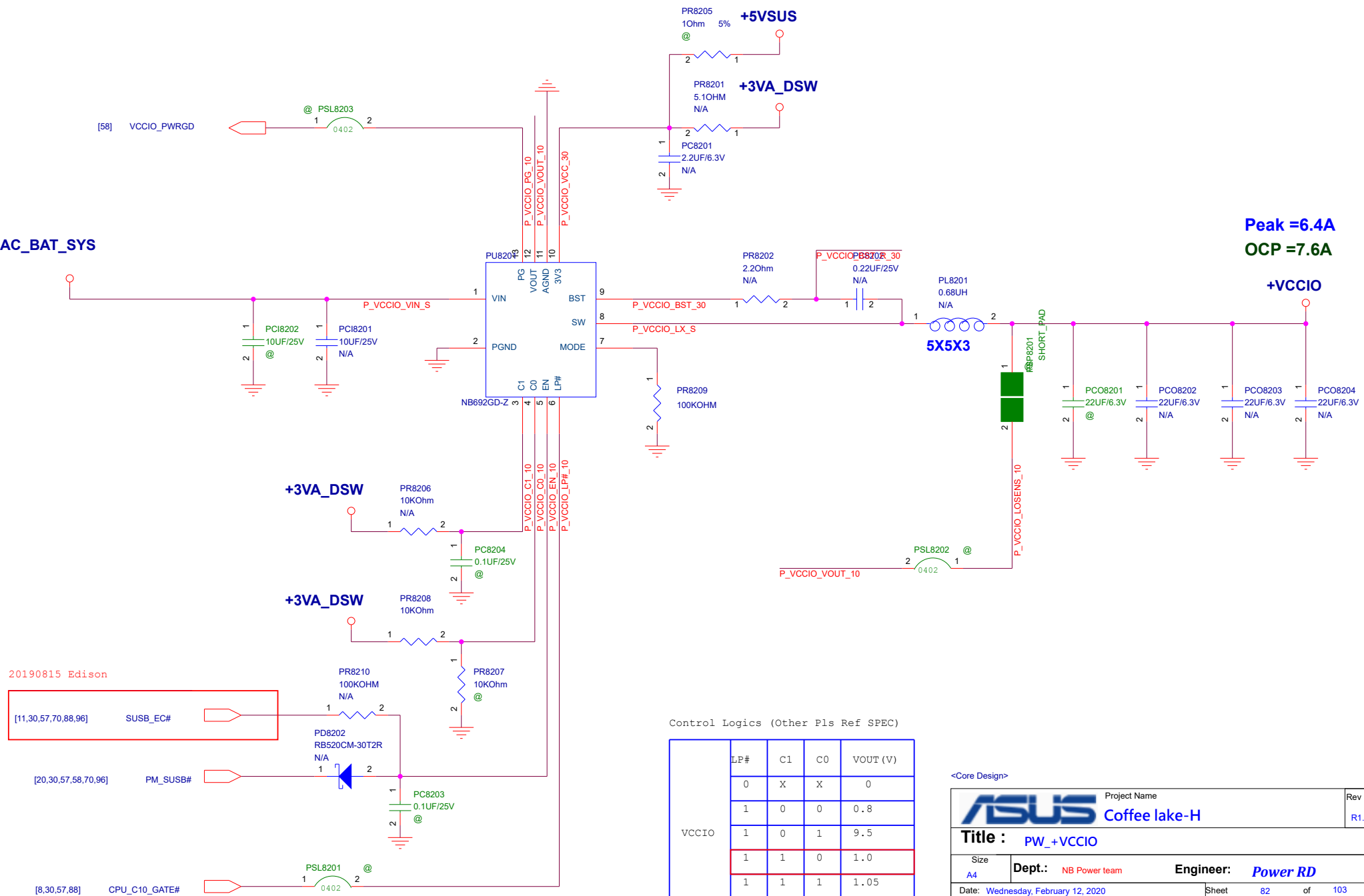






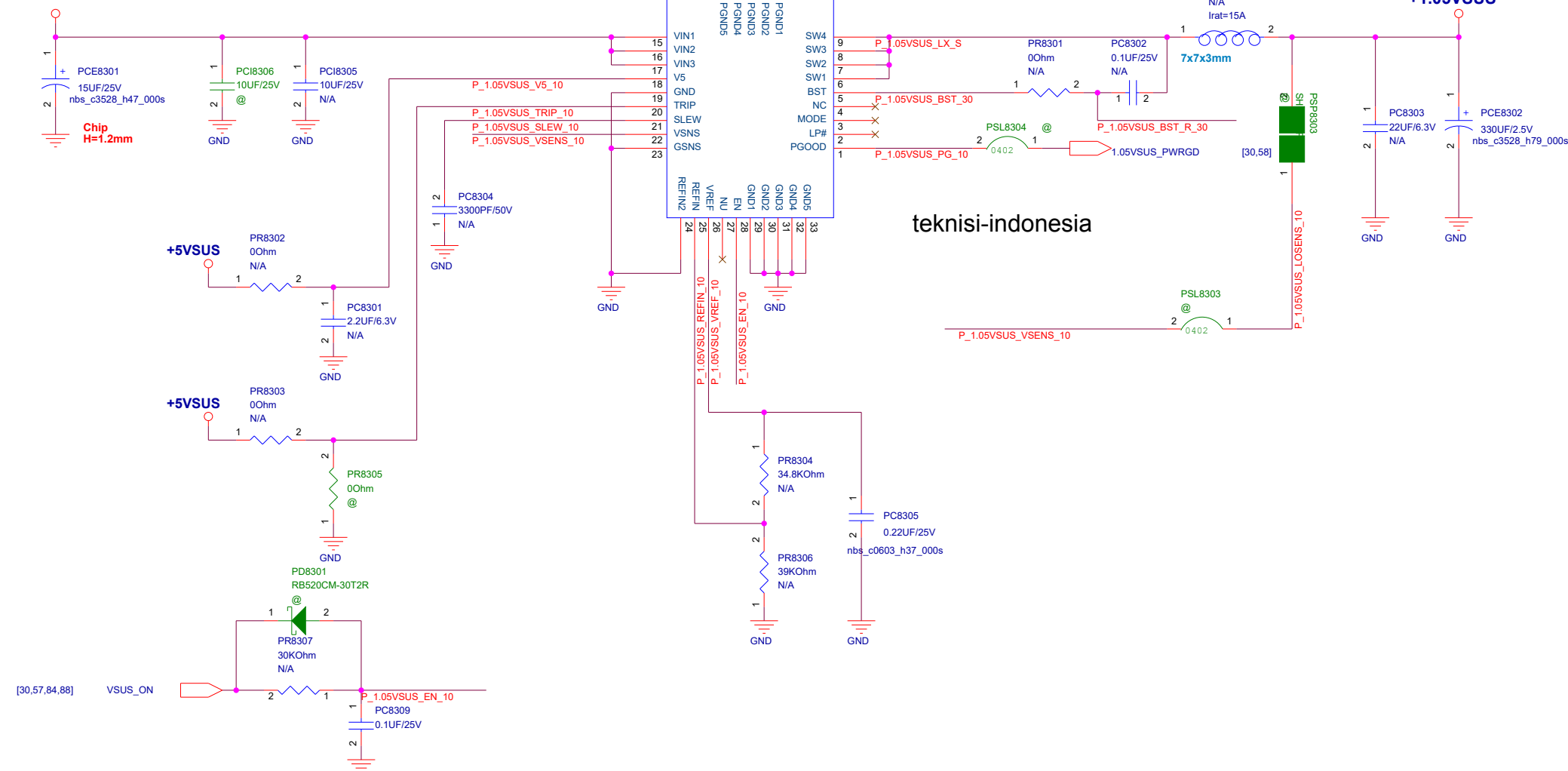


+VCCIO [For CPU]



+1.05VSUS [For PCH]

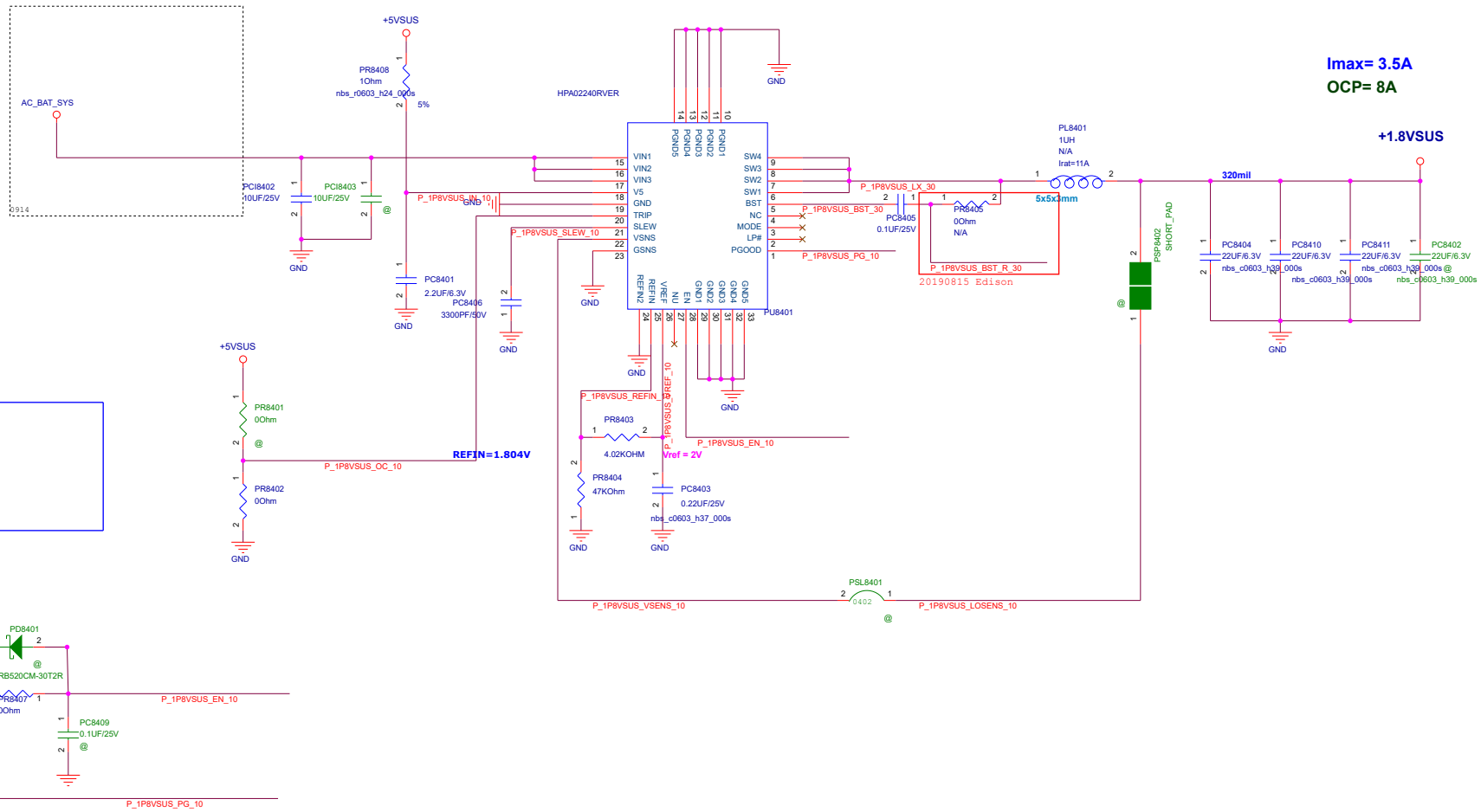
AC_BAT_SYS



PT840* 請放置 PU8401旁;並請放置Trace 上!



+1.8VSUS [For PCH]

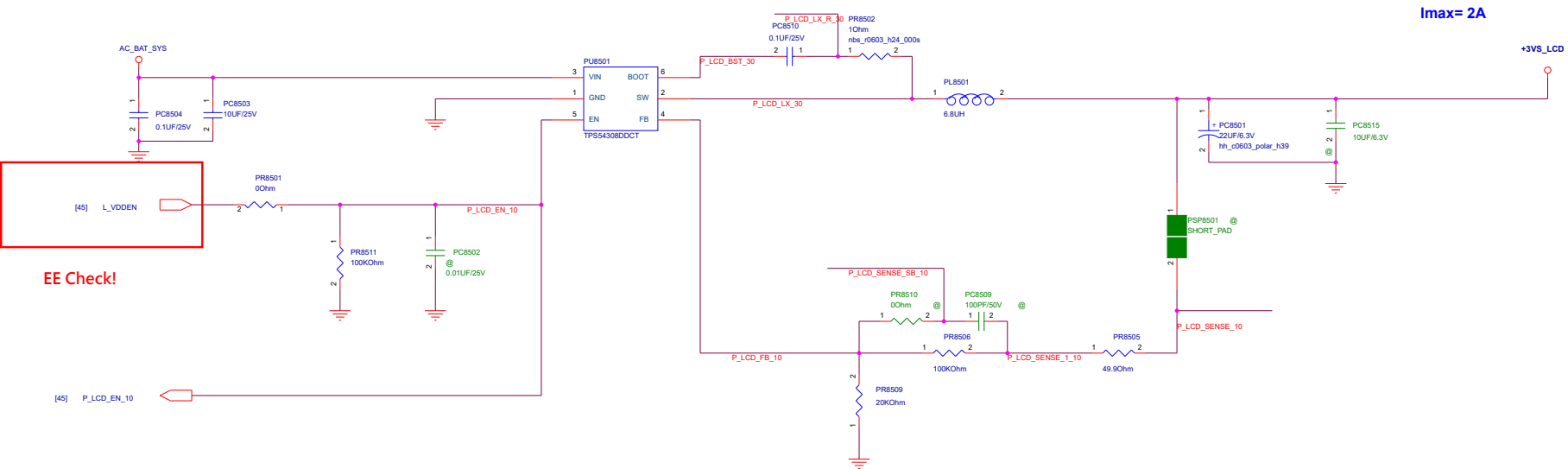


PT840* 請放置 PU8401旁;並請放置Trace 上!

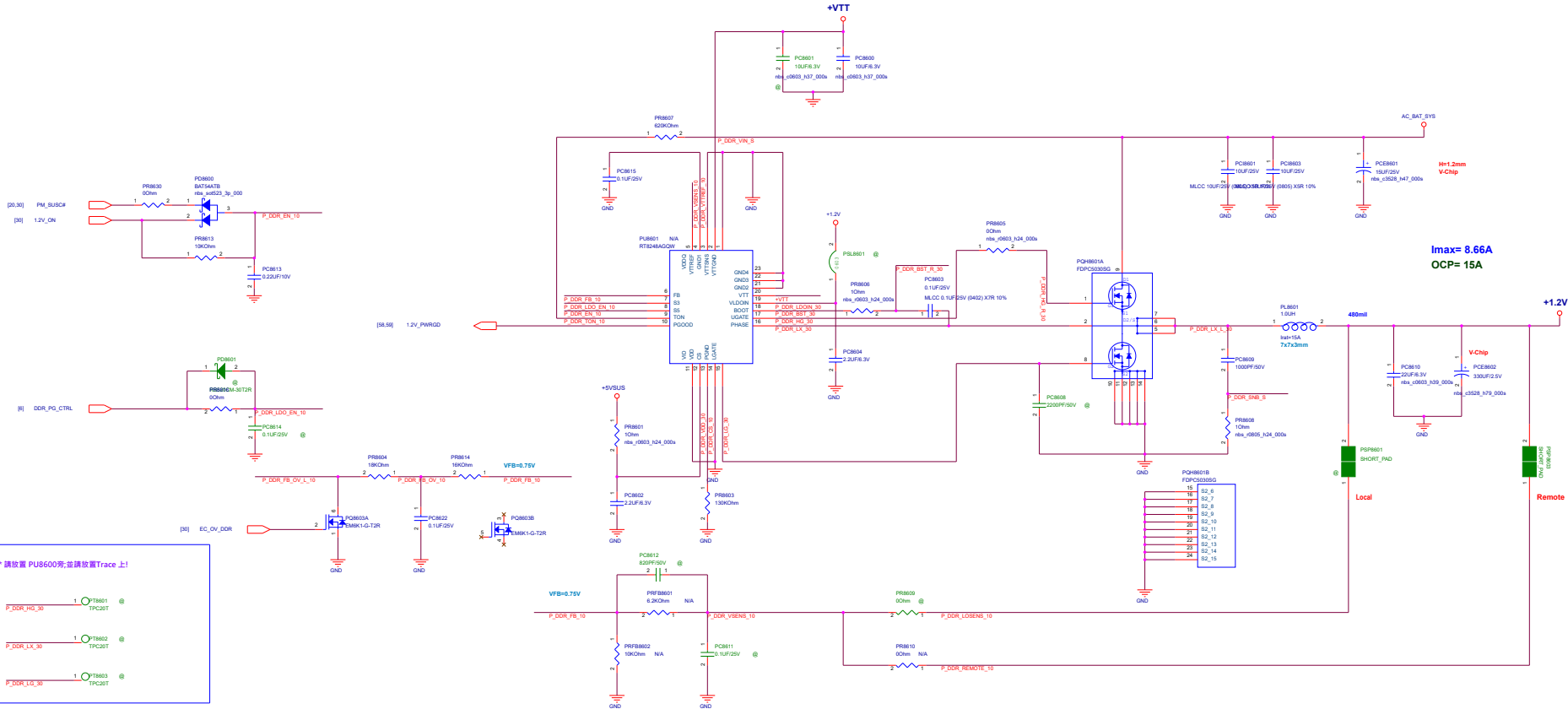
<Variant Name>

ASUS		Project Name	Rev
GX701			R1.0
Title : PW_+1.8VSUS			
Size	Dept.:	Engineer:	
A3	NB Power team	Power	
Date: Wednesday, February 12, 2020		Sheet	103

+3VS_LCD

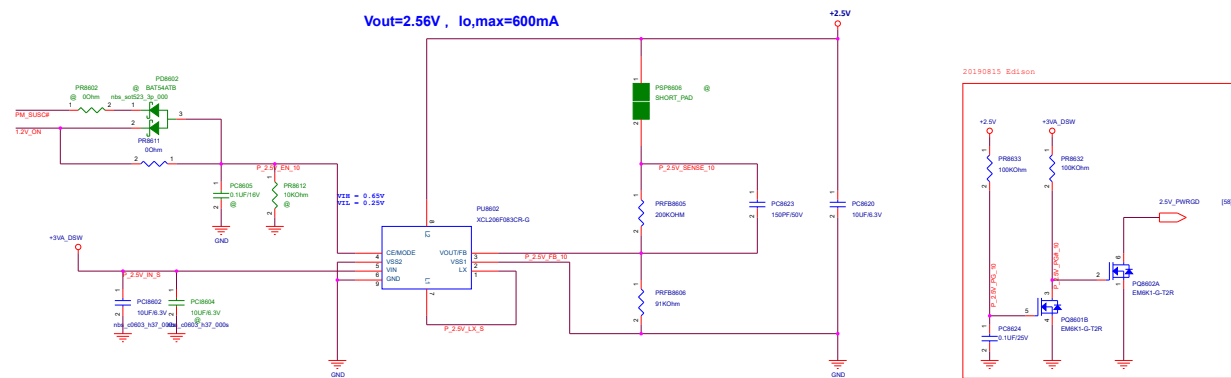


+1.2V / +VTT / +2.5V(For Memory)

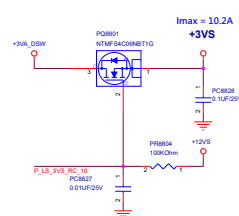
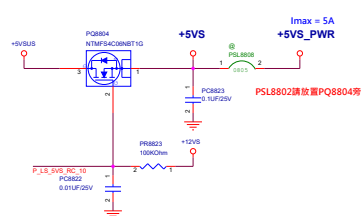
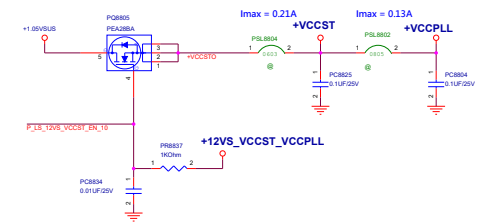
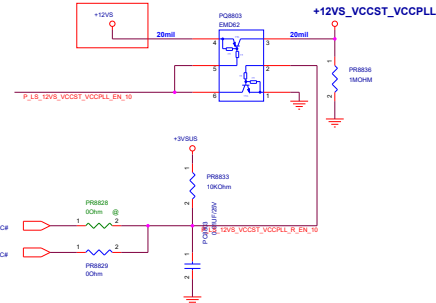
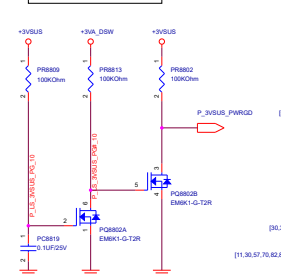
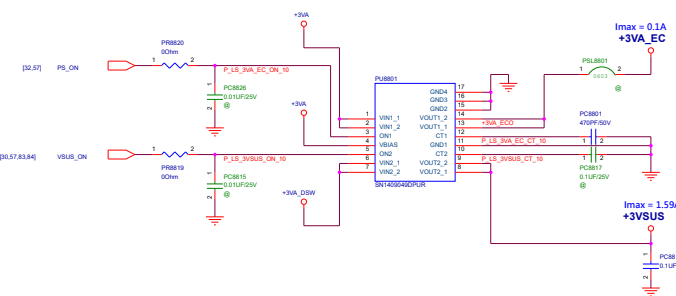


+2.5V BUCK (XCL206)

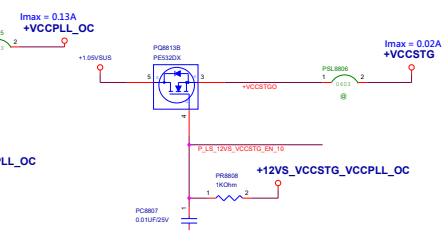
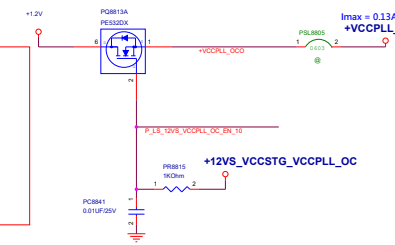
Vout=2.56V , I_{o,max}=600mA



Main Board

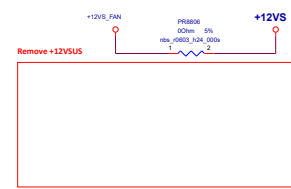


Remove VCCIO LS PWR rail 20190624

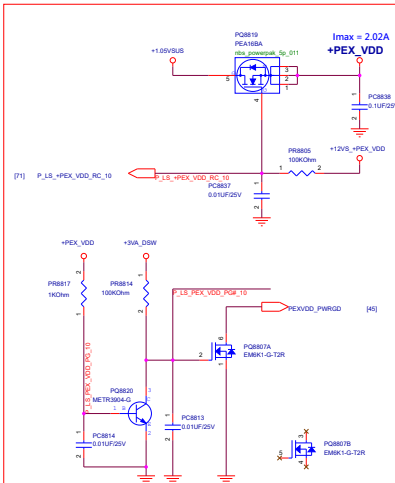
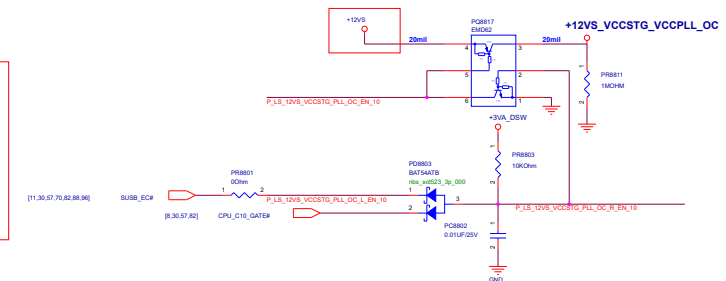


+12VS 的 Vin 對應 BOM 表

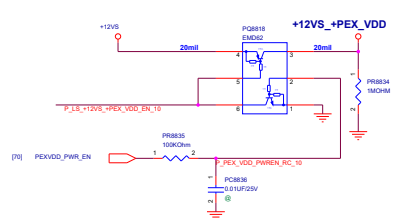
	+12V5_FAN	+12VSUS
PR8806	N/A	@
PR8810	@	N/A
PQ8814	@	N/A

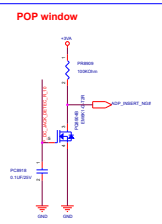
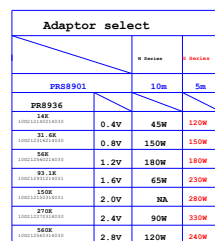
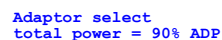


Remove +12VS_VCCIO L5 PWR rail 20190708

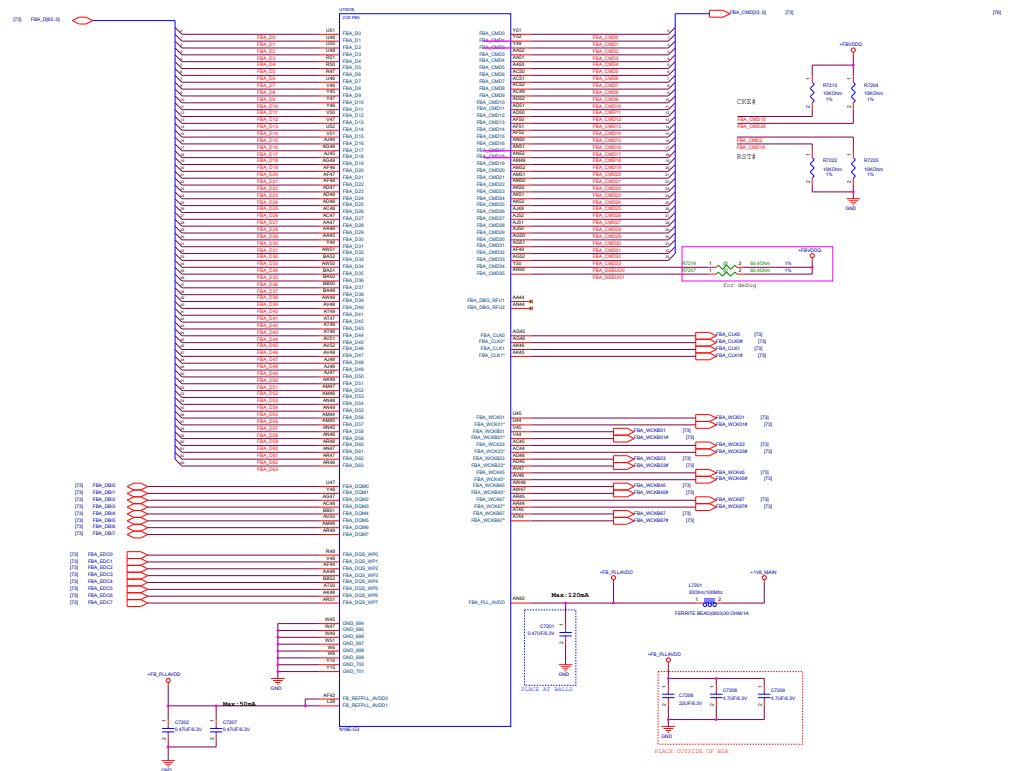


有獨立線路
P97: PW PEX VDD 時，
此處的線路請刪除

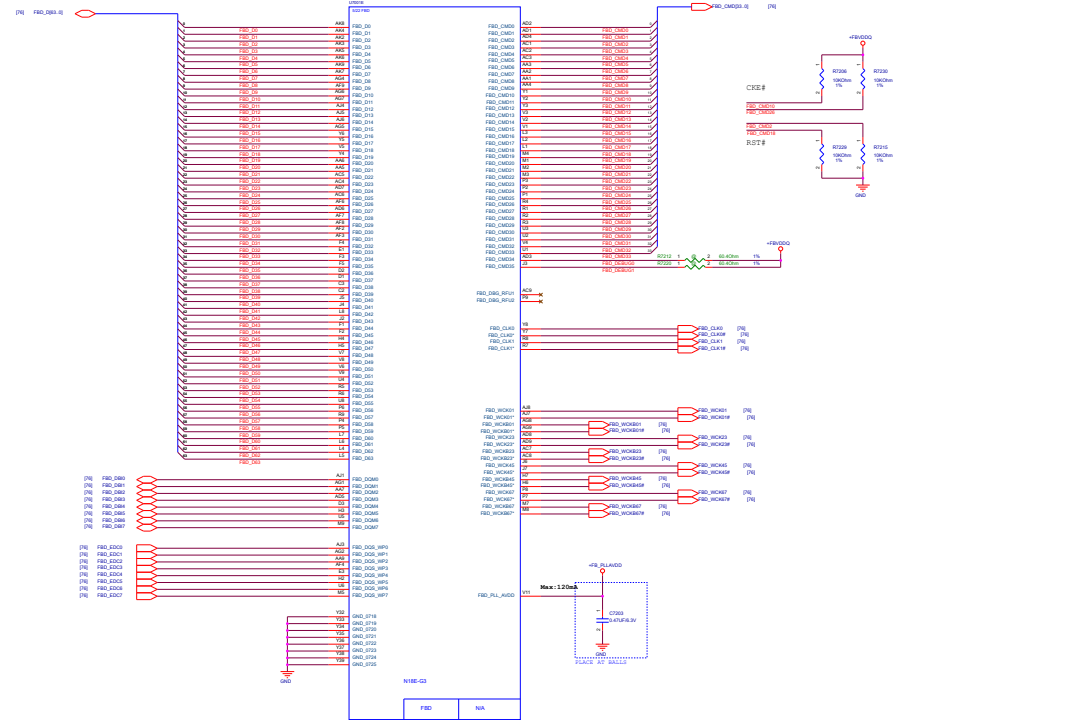




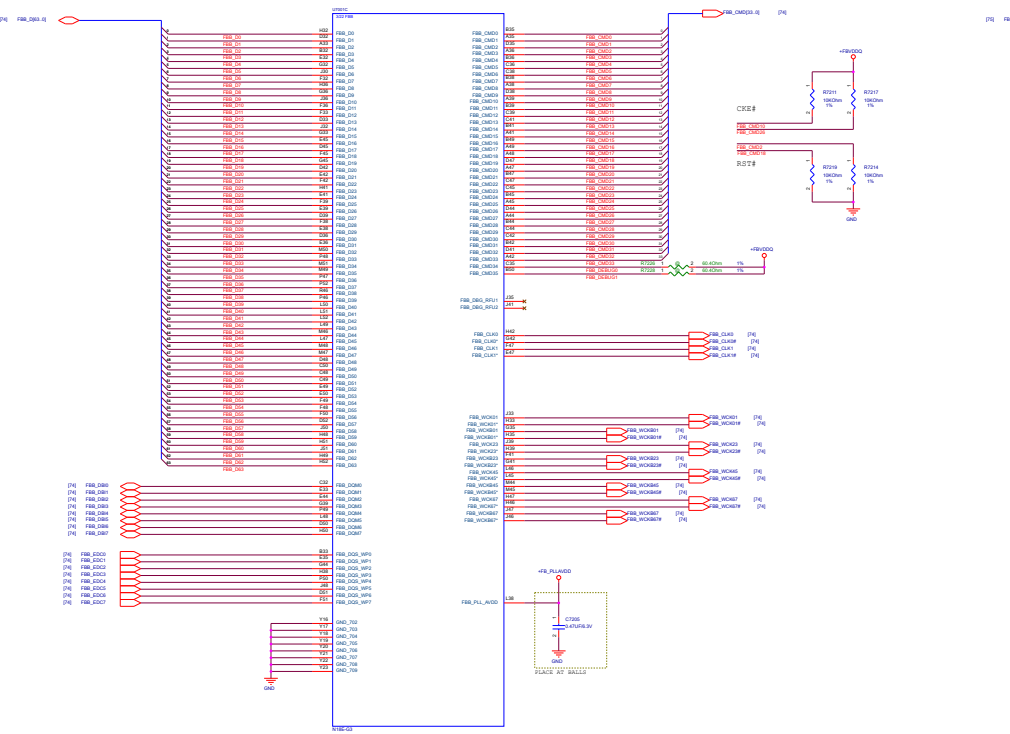
MEMORY: GPU FB Partition A



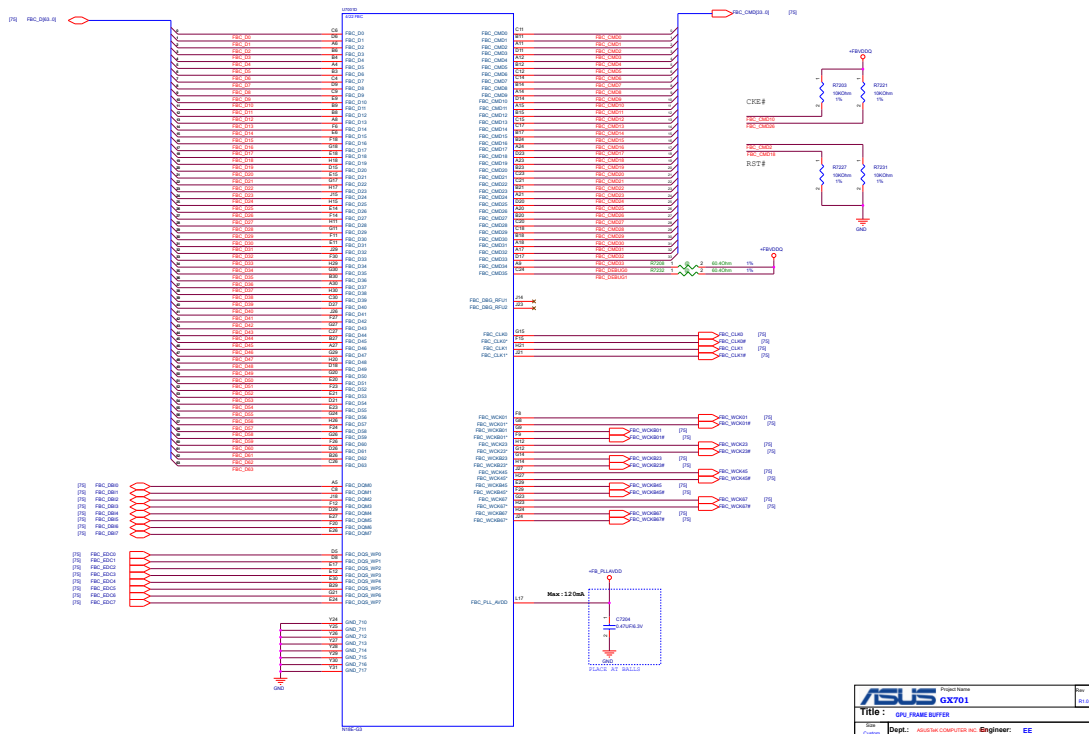
MEMORY: GPU FB Partition D

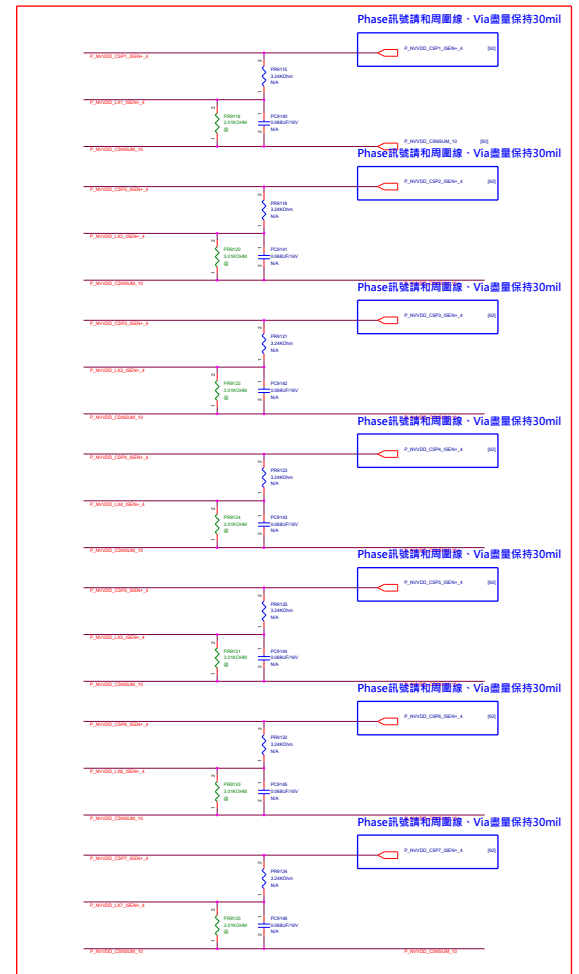
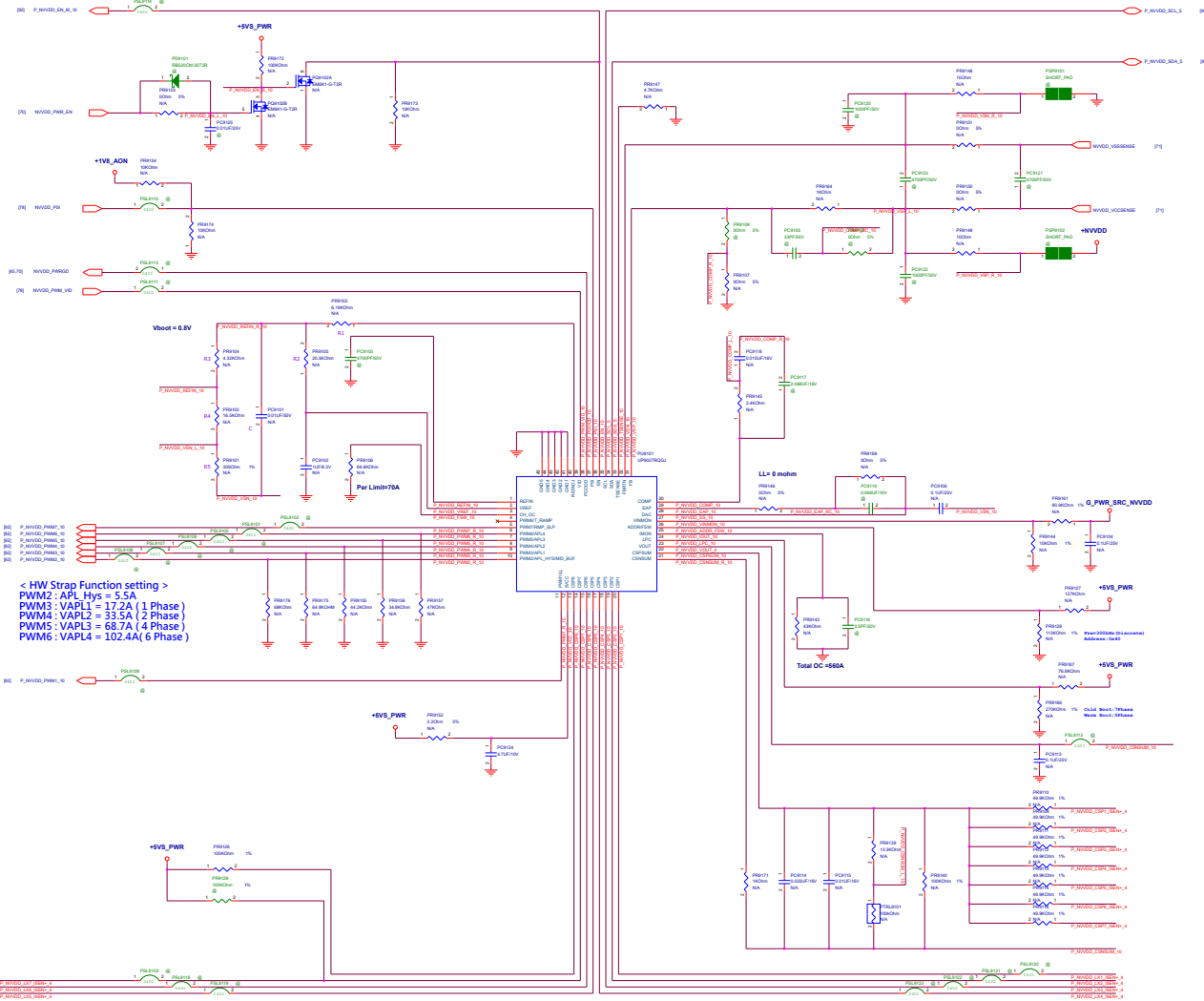


MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C

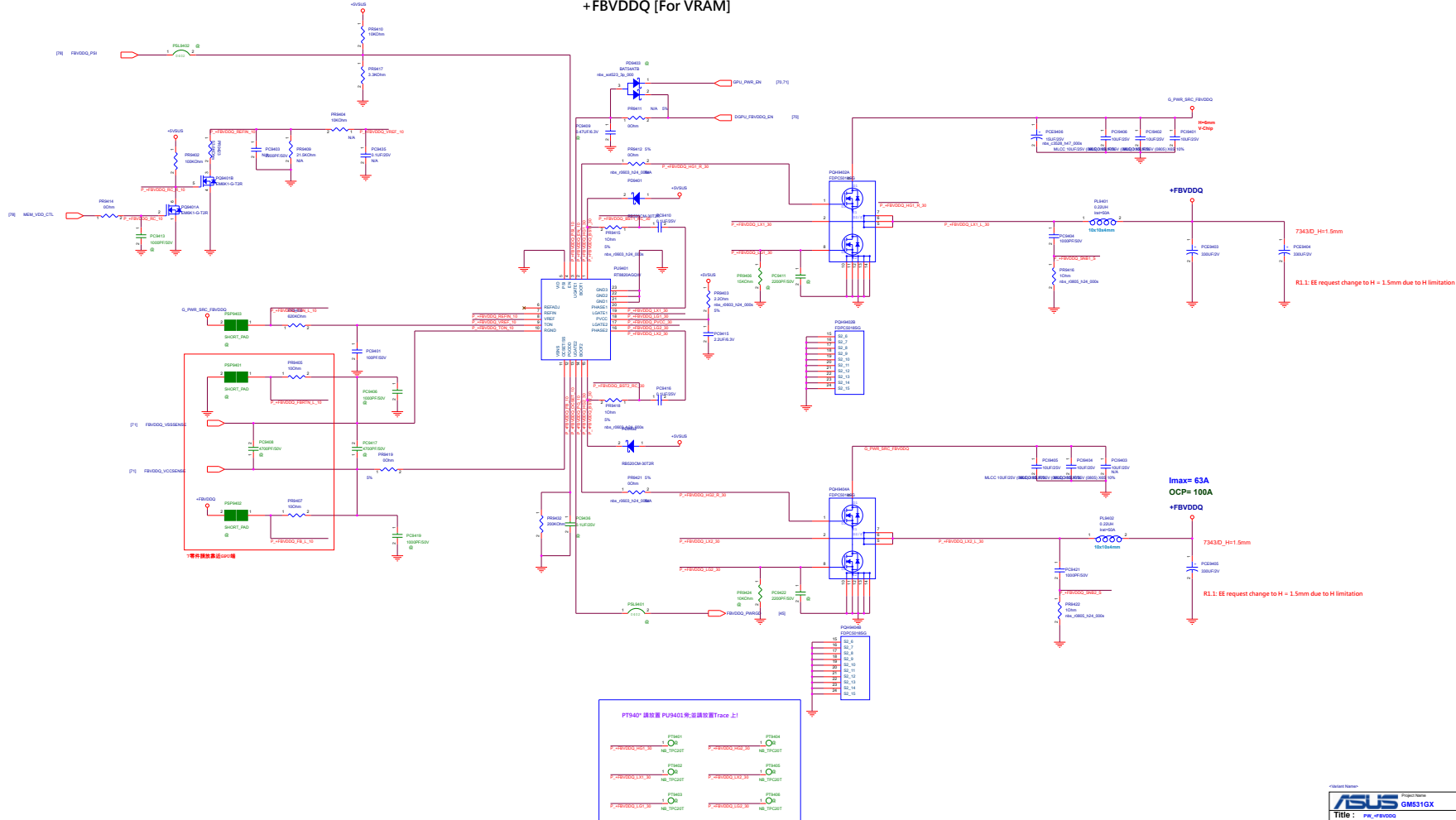




DVS Setting			
MDM_VDD_CTL	H	L	
Voltage	1.35V	1.2V	
PS0404	15000uA		
PS0409	21.5000uA		
PS0423	75000uA		

DVS Setting			
MDM_VDD_CTL	H	L	
Voltage	1.35V	1.2V	
PS0404	15000uA		
PS0409	21.5000uA		
PS0423	53.6000uA		

DVS Setting			
MDM_VDD_CTL	H	L	
Voltage	1.35V	1.2V	
PS0404	15000uA		
PS0409	16.5000uA		
PS0423	140000uA		



<Variant Name>



Project Name

Design IP R2.5

Rev

R2.5

Title : PW_ChargePump

Size

A2

Dept.: NB1-RD3EE1

Engineer: *CS Lin*

Date: Wednesday, February 12, 2020

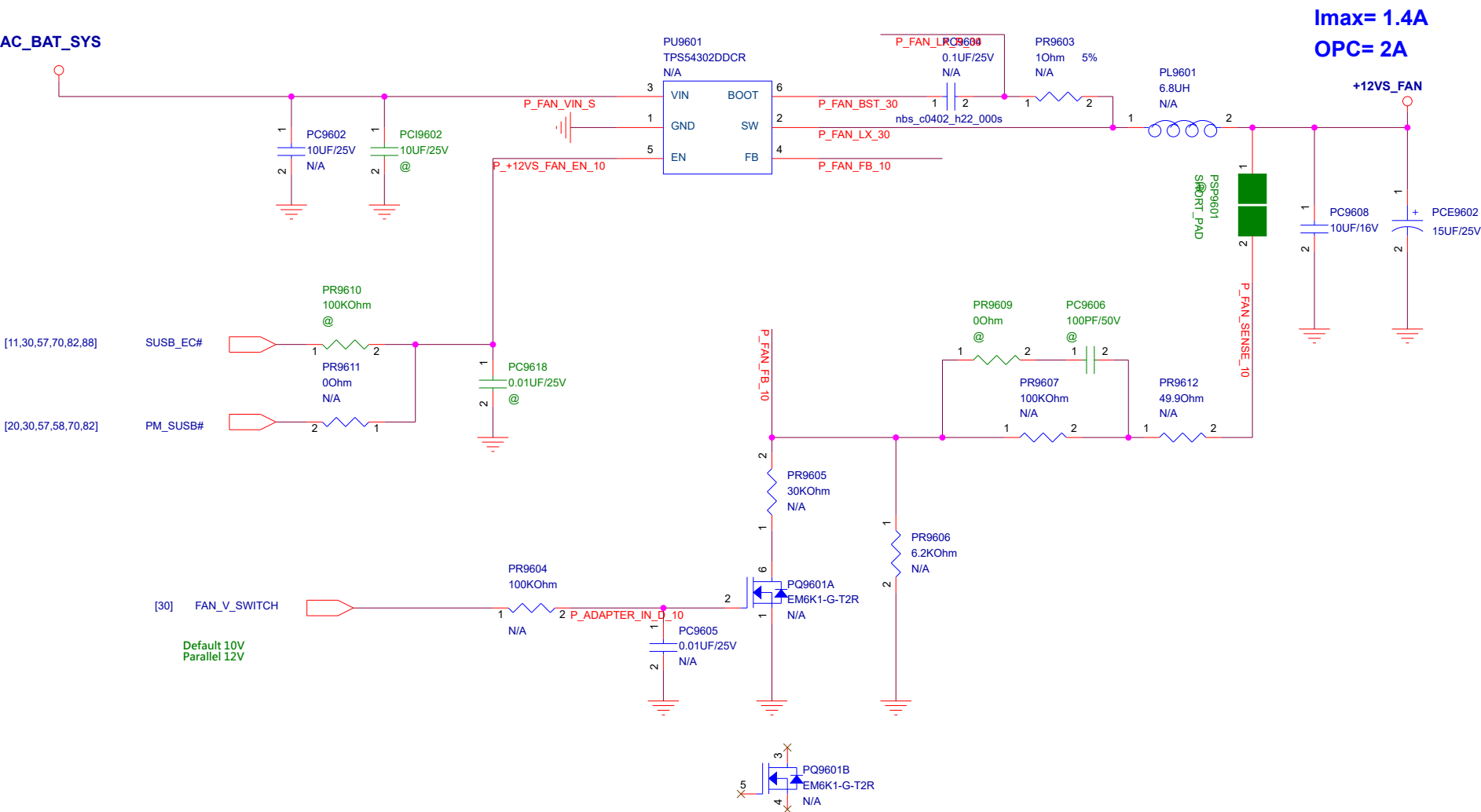
Sheet

95

of

103


+12VS_FAN [For FAN]

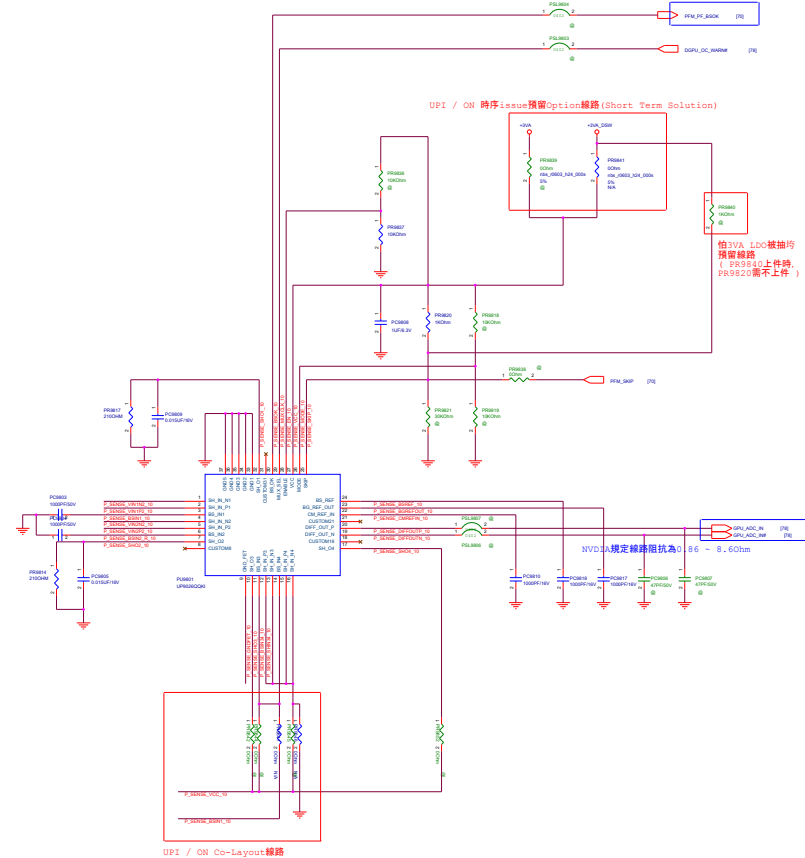
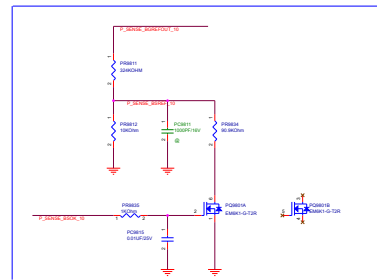
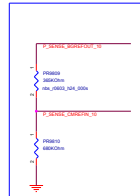
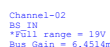
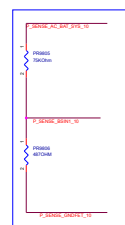
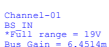
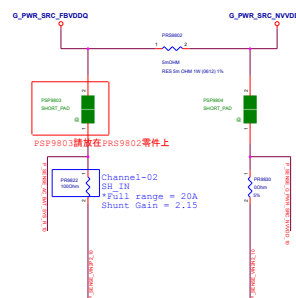
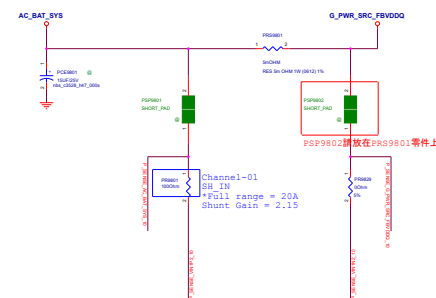


<Variant Name>

ASUS		Project Name	Rev
		Project Name	R1.0
Title : PW_+12VS_FAN			
Size A4	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, February 12, 2020	Sheet	96	of 103

<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size D	Project Name GX701		Rev 1.0
Date: Wednesday, February 12, 2020		Sheet 97 of 103	



N18E

N18E-G3/N18E-G3R

	U99026PQKI (UPI)	
PR9801	100q (10G212100014010)	
PR9817	124q (10G212124014010)	
PR9822	100q (10G212100014010)	
PR9814	124q (10G212124014010)	
PR9805	75kq (10G212750214010)	
PR9806	487q (10G212487014010)	
PR9807	75kq (10G212750214010)	
PR9808	487q (10G212487014010)	
PR9811	524kq (10G21324314010)	
PR9812	100kq (10G212100214010)	
PR9834	90.9kq (10G212909214010)	

N18E-G2/N18E-G2R
N18E-G1R

[illegible]

N18E-G0
N18E-G1
N18E-G3R MAX-Q
N18E-G2R MAX-Q
N18E-G1R MAX-Q

[illegible]

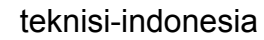
N18E-G0 MAX-Q

[illegible]

N18P

	UP9026PQKI (UPI)	
PR9801	100g (10G212100014010)	
PR9817	348g (10G212348014030)	
PR9822	100g (10G212100014010)	
PR9814	348g (10G212348014030)	
PR9805	75kg (10G212750214010)	
PR9806	487g (10G212487014010)	
PR9807	75kg (10G212750214010)	
PR9808	487g (10G212487014010)	
PR9811	324kg (10G21324314010)	
PR9812	10kg (10G212100214010)	
PR9834	90.9kg (10G212909214010)	

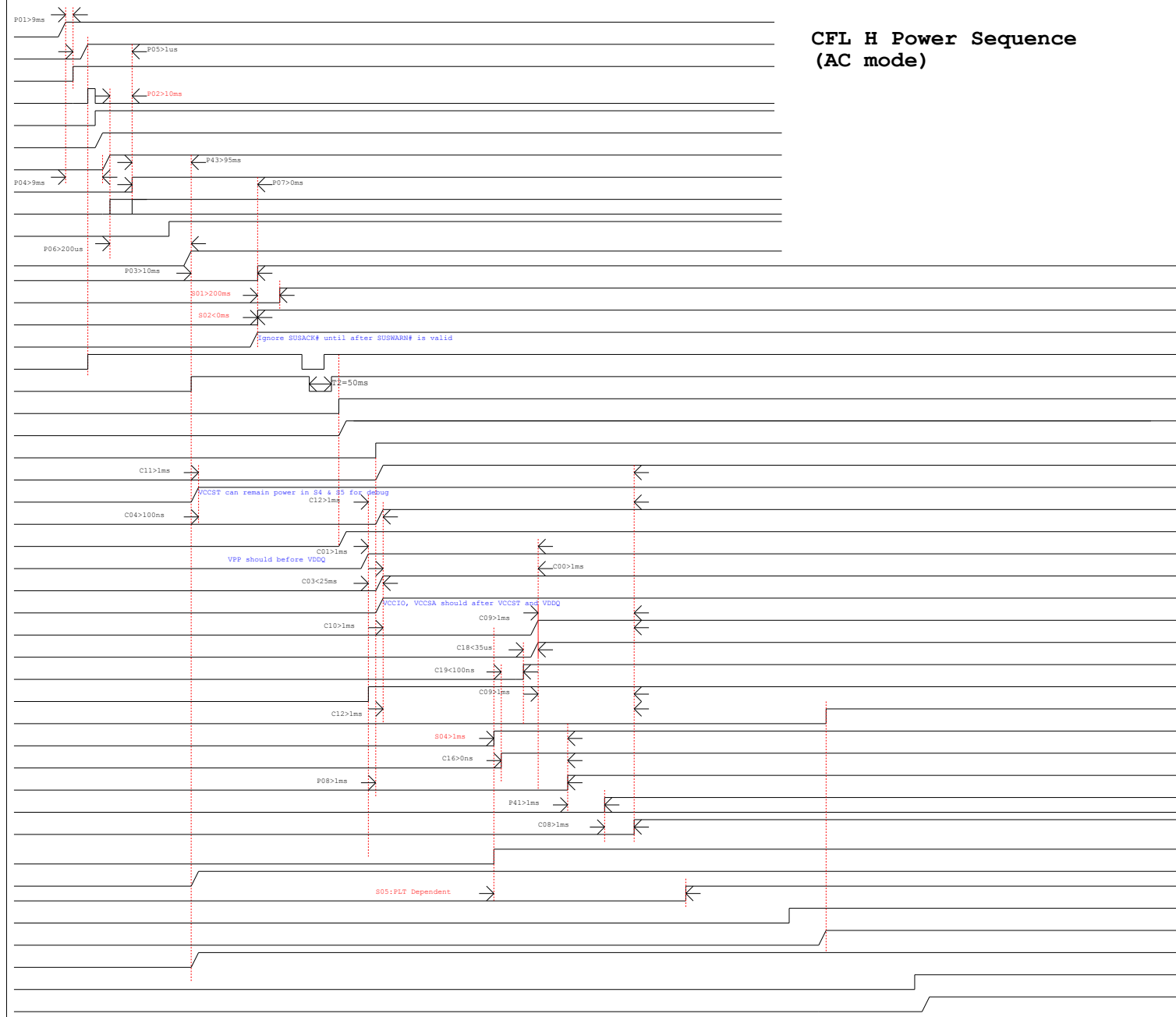
N18P-G0-MP
N18P-G0-MP MAX-Q
N18P-G0-Q13 MAX-Q
N18P-G62
N18P-G62 MAX-Q
N18P-G61
N18P-G61 MAX-Q



```

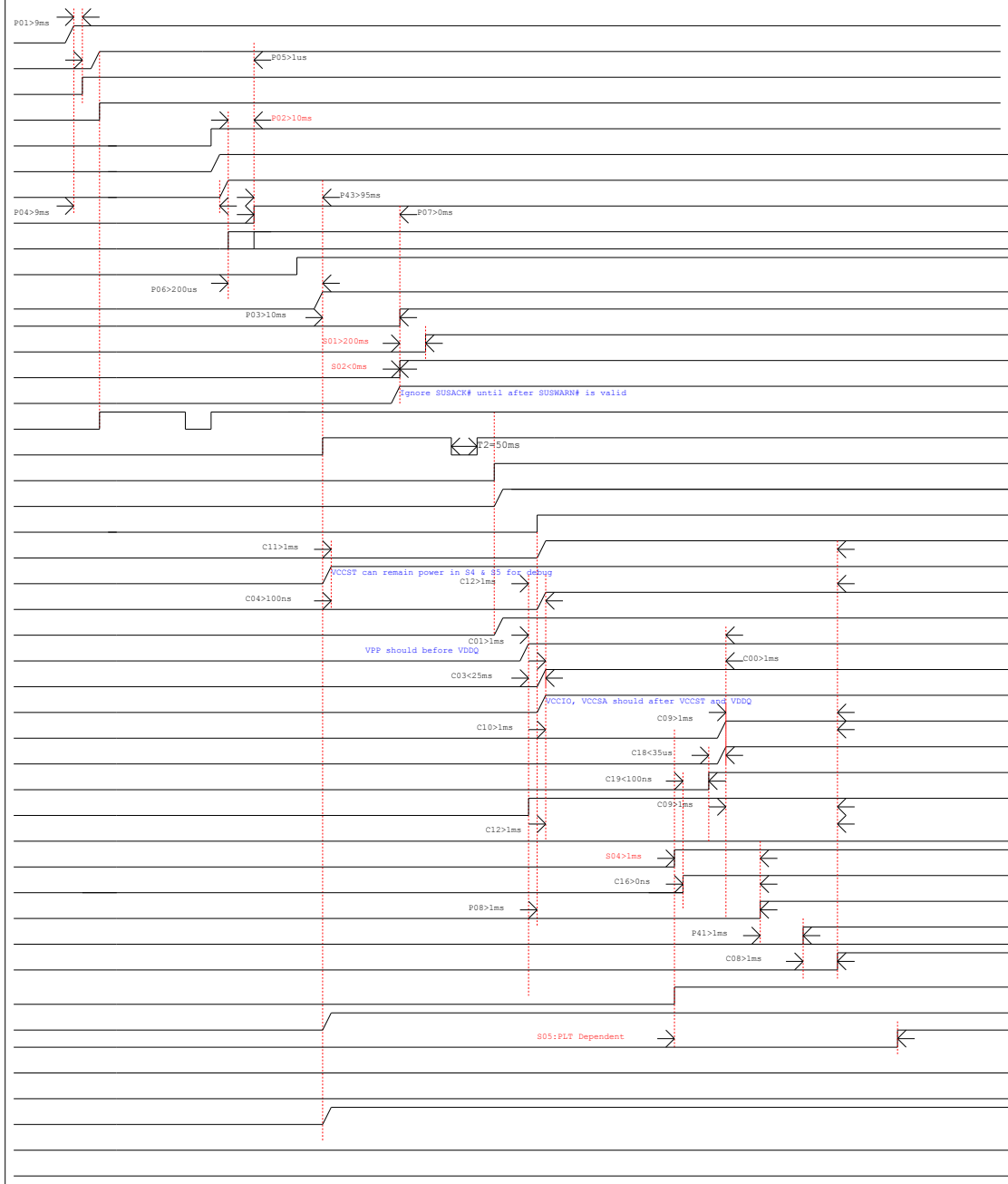
C:CPU                                     (+RTCBAT)+3VA_RTC
P:PCH                                     (AC_BAT_SYS)+3VA/+5VA
S:PLT                                     (+3VA_RTC) RTCRST# (PCH)
Power                                     (Power) AC_IN_OC# (EC)
Signal                                   (EC) PS_ON (+3VA_EC)
                                           (PS_ON)+3VA_EC (EC)
                                           (3VADSW_ON)+3VA_DSW (3VA_DSW_FWRGD)
                                           (EC) DFWROK_EC (PCH)
                                           (+3VA_DSW) PM_BATLOW# (PCH)
                                           (PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_FWRGD)
                                           (EC) PM_RSMRST#_PCH (PCH)
                                           (PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
                                           (EC) PCH_SUSACK# (PCH)
                                           (PWR_Switch) PWR_SW# (EC)
                                           (EC) PM_FWRBTN# (PCH)
                                           (EC) SUSC_EC# (Power)
                                           (SUSC_EC#)+12V/+5V/+3V
                                           (EC) SUSB_EC# (Power)
                                           (SUSB_EC#)+12VS/+5VS/+3VS
                                           (SUSB_EC#)+1.0V_VCCST, VCCPLL
                                           (SUSB_EC#)+VCCIO, (+12VS)+VCCSTG
                                           (1.2V_ON)+2.5V (2.5V_FWRGD)
                                           (1.2V_ON)+VDDQ_CPU (1.2V_FWRGD)
                                           (+12VS)+VCCPLL_OC
                                           (SUSB_EC#)+VCCIO (VCCIO_FWRGD)
(ALL_SYSTEM_FWRGD)+VCCSA (IMVP8_FWRGD)
                                           (DDR_VTT_CTRL)+0.6V
                                           (CPU) DDR_VTT_CTRL (Power)
                                           (Power) 1.2V_FWRGD (AND)
                                           (Power) IMVP8_FWRGD
(AND) ALL_SYSTEM_FWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_FWRGD) VCCST_FWRGD_CPU (CPU)
                                           (EC) PM_FWROK_PCH (PCH)
                                           (PCH) CLK_PCH_BCLK (CPU)
                                           (PCH) H_CPUFWRGD (CPU)
                                           (CPU) P_SVID_DATA_X2 (Power)
                                           (EC) PM_SYSPWROK_PCH (PCH)
                                           (PCH) PLT_RST# (CPU/EC/Device)
                                           (P_IMVP8_DRVON)+VCCCORE (IMVP8_FWRGD)
                                           (CPU) H_THERMTRIP# (PCH)
                                           (PCH) DDR4_DRAMRST# (Memory)
                                           +VCCIO

```



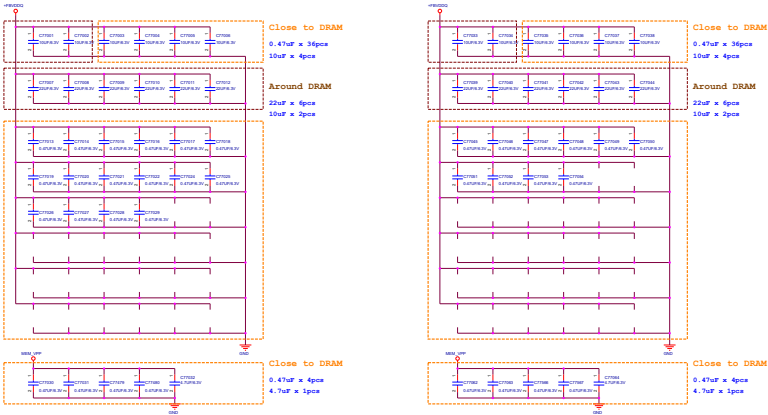
DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
 P:PCH (AC_BAT_SYS)+3VA/+5VA
 S:PLT (+3VA_RTC) RTCRST# (PCH)
 Power (Power) AC_IN_OC# (EC)
 Signal (EC) PS_ON (+3VA_EC)
 (PS_ON)+3VA_EC (EC)
 (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
 (EC) DPWROK_EC (PCH)
 (+3VA_DSW) PM_BATLOW# (PCH)
 (PCH) PM_SLP_SUS# (EC)
 (VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
 (EC) PM_RSMRST#_PCH (PCH)
 (PCH) SUSWARN# (EC)
 (EC) ME_AC_PRESENT_PCH (PCH)
 (EC) PCH_SUSACK# (PCH)
 (PWR_Switch) PWR_SW# (EC)
 (EC) PM_PWRBTN# (PCH)
 (EC) SUSC_EC# (Power)
 (SUSC_EC#)+12V/+5V/+3V
 (EC) SUSB_EC# (Power)
 (SUSB_EC#)+12VS/+5VS/+3VS
 (VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
 (+VCCIO)+VCCSTG
 (1.2V_ON)+2.5V (2.5V_PWRGD)
 (1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
 (+12VS)+VCCPLL_OC
 (SUSB_EC#)+VCCIO (VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU) DDR_VTT_CTRL (Power)
 (Power) 1.2V_PWRGD (AND)
 (Power) IMVP8_PWRGD
 (AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
 (EC) PM_PWROK_PCH (PCH)
 (PCH) CLK_PCH_BCLK (CPU)
 (PCH) H_CPU_PWRGD (CPU)
 (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
 (CPU) P_SVID_DATA_X2 (Power)
 (EC) PM_SYSPWROK_PCH (PCH)
 (PCH) PLT_RST# (CPU/EC/Device)
 (P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
 (CPU) H_THERMTRIP# (PCH)
 (PCH) DDR4_DRAMRST# (Memory)
 +VCCGT

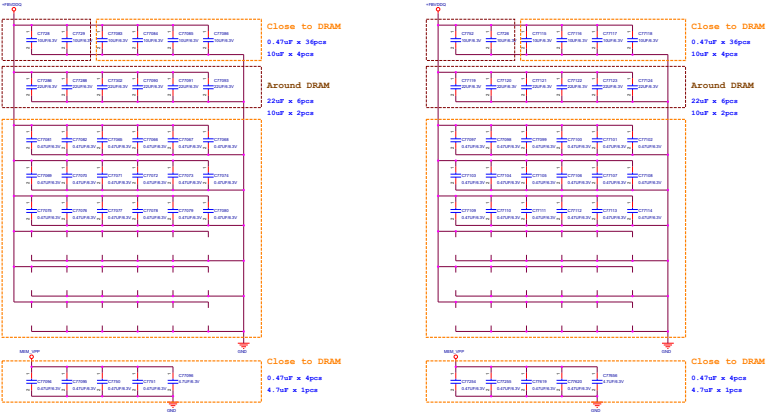


CFL H Power Sequence (DC mode)

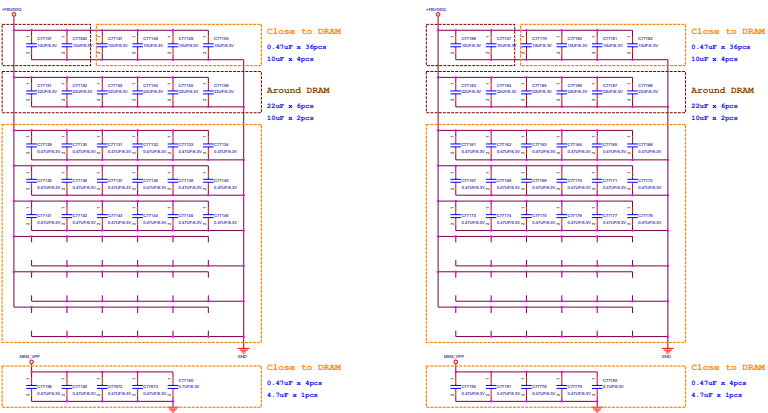
Channel A



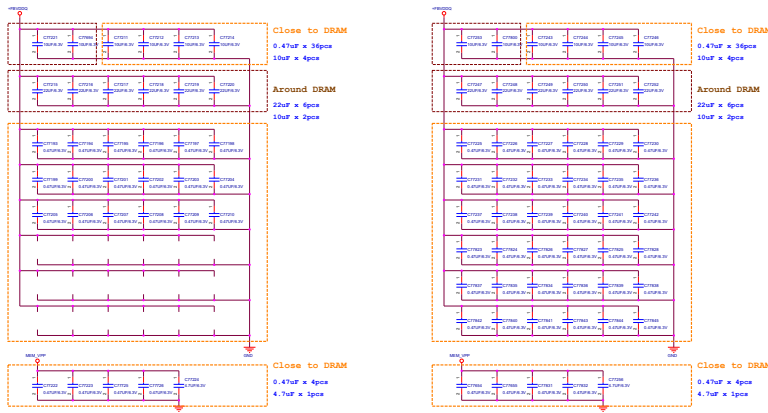
Channel B



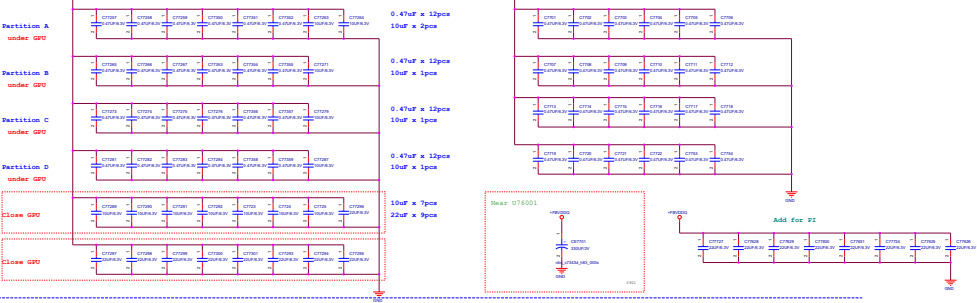
Channel C



Channel D



VRAM PWR_FBVDQ



For power sequence measurement

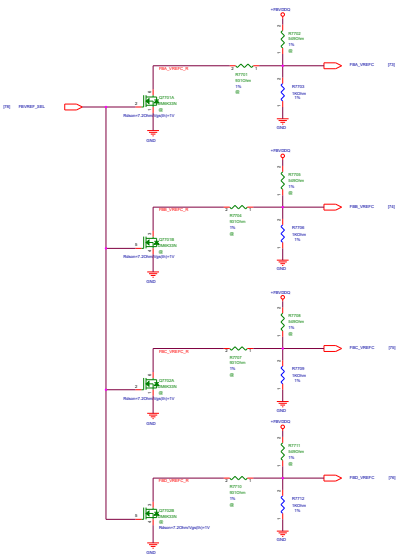


Address Selection Table

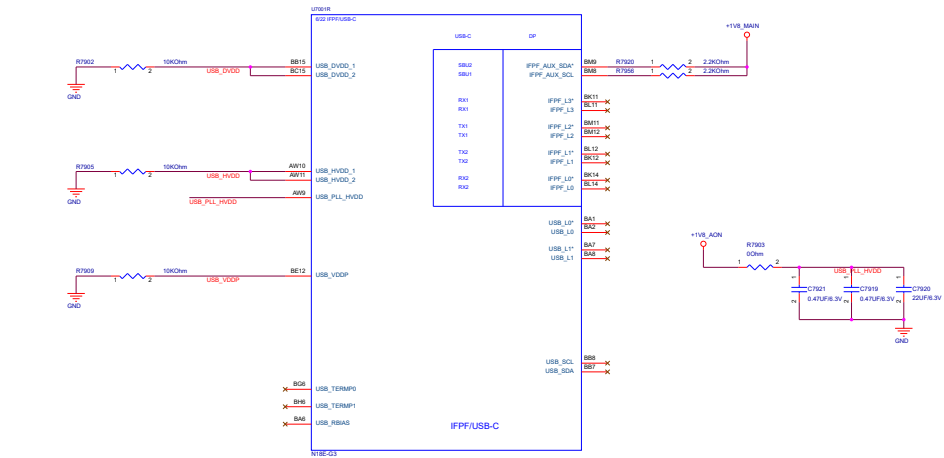
Address	Bank	Row	Column	Value
0000	0	0	0	0
0001	0	0	1	1
0002	0	0	2	2
0003	0	0	3	3
0004	0	0	4	4
0005	0	0	5	5
0006	0	0	6	6
0007	0	0	7	7
0008	0	0	8	8
0009	0	0	9	9
000A	0	0	10	10
000B	0	0	11	11
000C	0	0	12	12
000D	0	0	13	13
000E	0	0	14	14
000F	0	0	15	15

GL702VSK UP1905

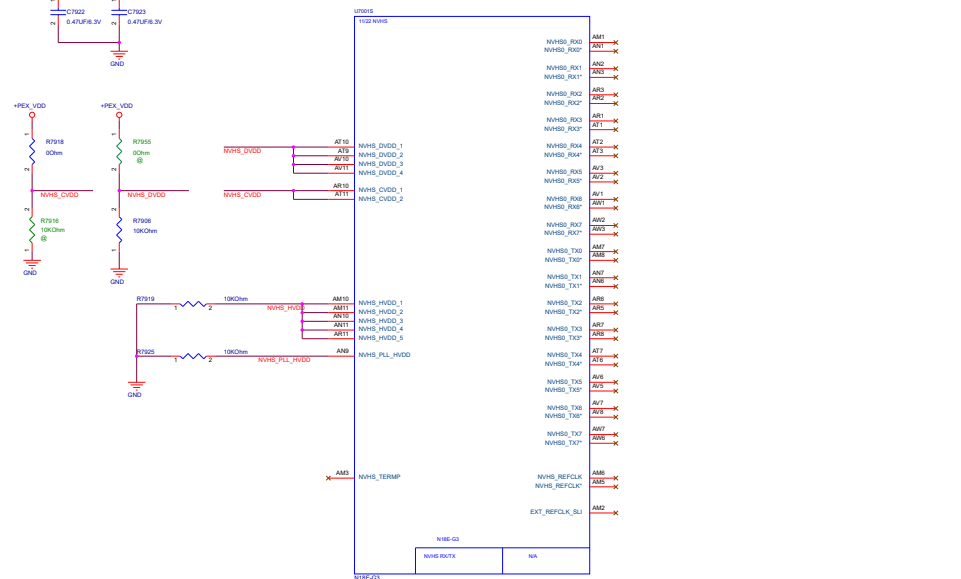
移至 Page 50



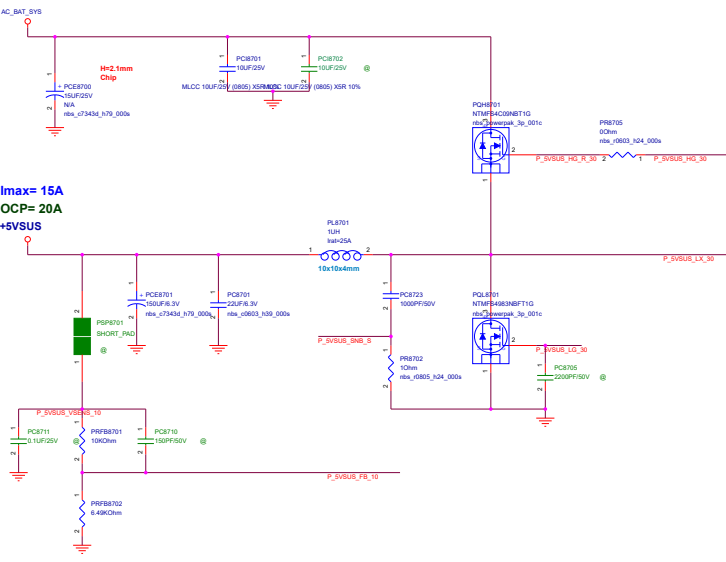
Main Board



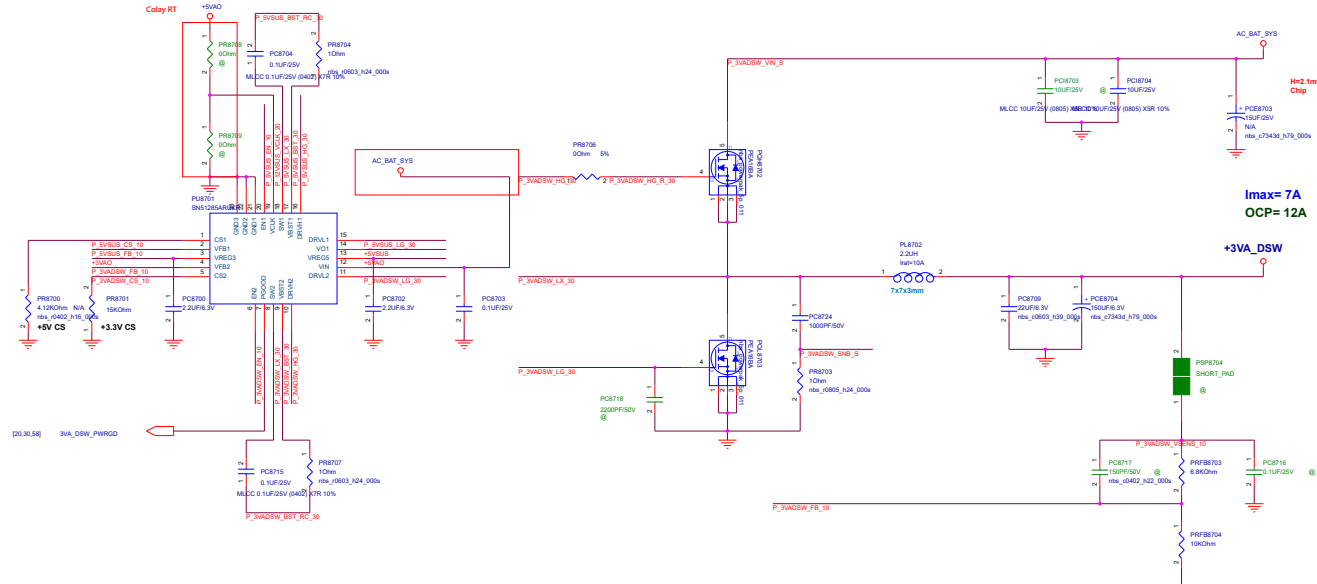
HDMI & DP



+3VA_DSW / +5VSUS [System Power]



Imax= 15A
OCP= 20A
+5VSUS



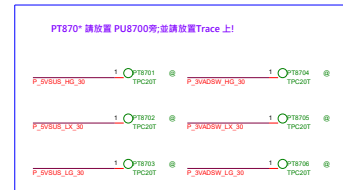
Imax= 7A
OCP= 12A
+3VA_DSW

Remove charge pump

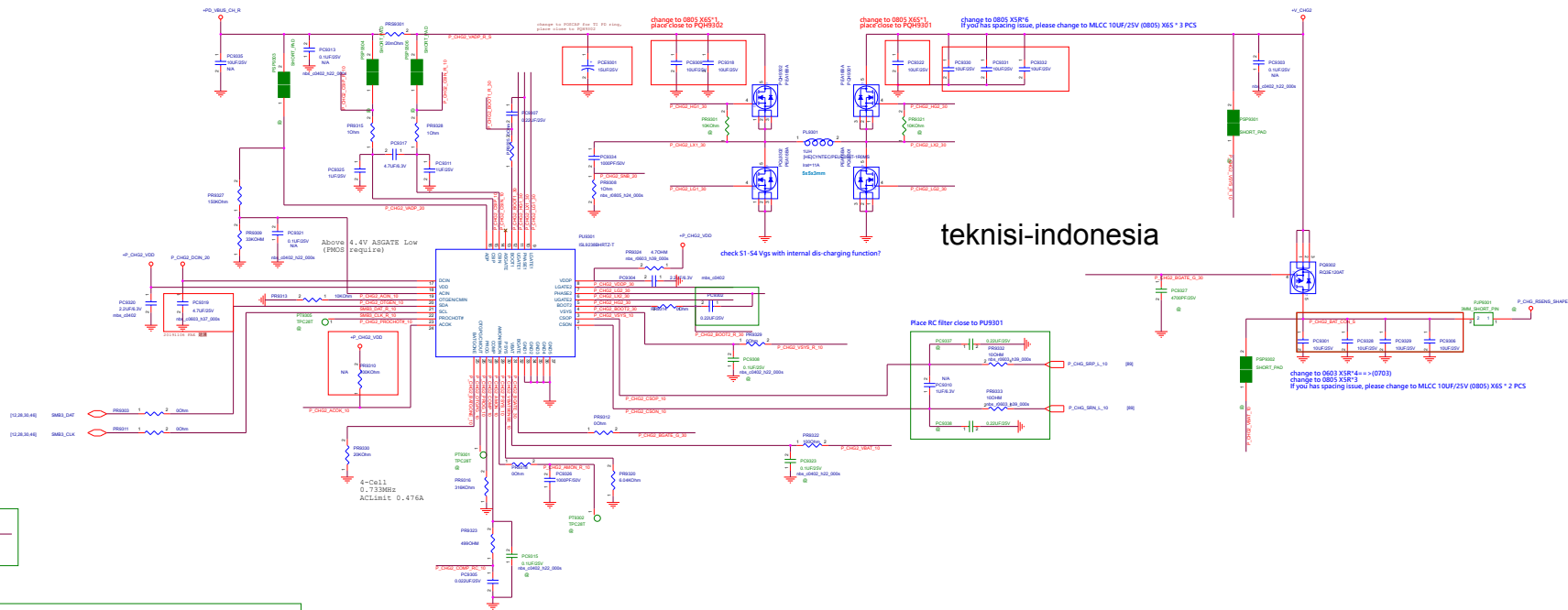


Adaptor Mode (IMVP8)							
	S0	C5	S3	D33	S4	S5	S5 with USB Charge+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP5)							
	S0	C5	S3	D33	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



Charger ISL9238 (NVDC)

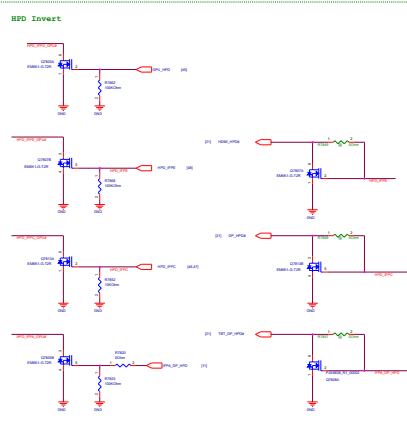


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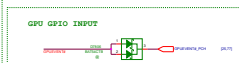
```
Strap 0X0 - GDOR6 Samsung
Strap 0X1 - GDOR6 Micron
```



Level shift



VGA EXT. Thermal Sensor



```
NVIDIA_GCS 2.0 follow DG-07290-001_v01
GPU_GPD5 -> FRAME_LOCK# (input, Open Drain)
High -> driver display / Low Normal
```

FRAME_LOCK# @ Pull High + PFE_LCD at Panel side

CHAPTER 12.3

Single Prng Pass Test			RANGLS Setting Number			Single Prng Pass Test			Convergence Rate (No. Trials)				
STRAP2	STRAP1	STRAP3	(see Memory Test for memory config. parameters)	STRAP2	STRAP1	STRAP3	(see Memory Test for memory config. parameters)	STRAP2	STRAP1	STRAP3	STRAP2	STRAP1	STRAP3
L	L	L	0.000000	L	H	L	14 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	15 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	16 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	17 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	18 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	19 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	20 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	21 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	22 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	23 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	24 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	25 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	26 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	27 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	28 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	29 (0.000000)	L	L	L	1	1	1
L	L	L	0.000000	H	H	L	30 (0.000000)	L	L	L	1	1	1

[illegible]